Honeywell

Ultrafast and Nanoscale Optics Group
UNIVERSITY OF CALIFORNIA, SAN DIEGO

Optically Programmable FPGA Systems

Demetri Psaltis

California Institute of Technology

Partners

Holoplex

Honeywell

University of California, San Diego

Photobit

HOLOPLEX

DARPA
MTO

Optically Programmable FPGA Systems

Goals:

- Demonstrate a parallel optical interface between a holographic memory and a silicon circuit
- Apply the unique capabilities of the OPGA to image processing, recognition and database search.

Approach:

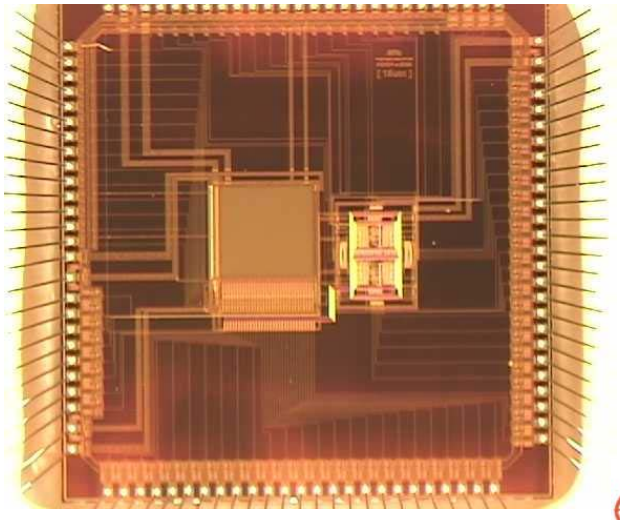
Combine in a compact OPGA Module:

- **VLSI chip containing logic & detectors**
- **Holographic memory**
- **VCSEL array**

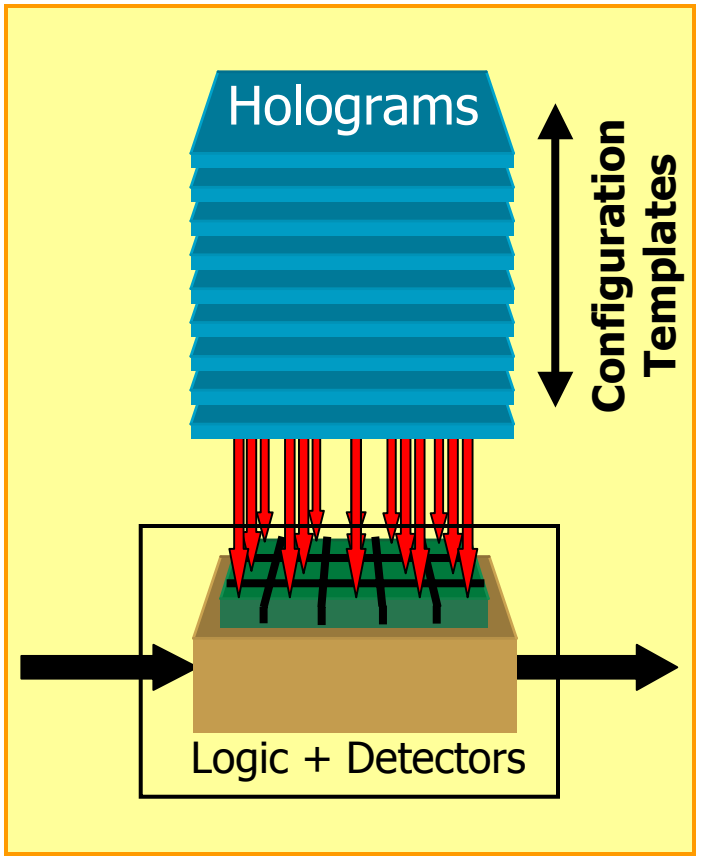
Achievements:

- **Demonstration of optically reconfigurable logic circuits**
- **100 Holographic reconfiguration templates**
- **VCSEL's and MEMS addressing**
- **Compact module integrating VCSELs, Holograms and Silicon**

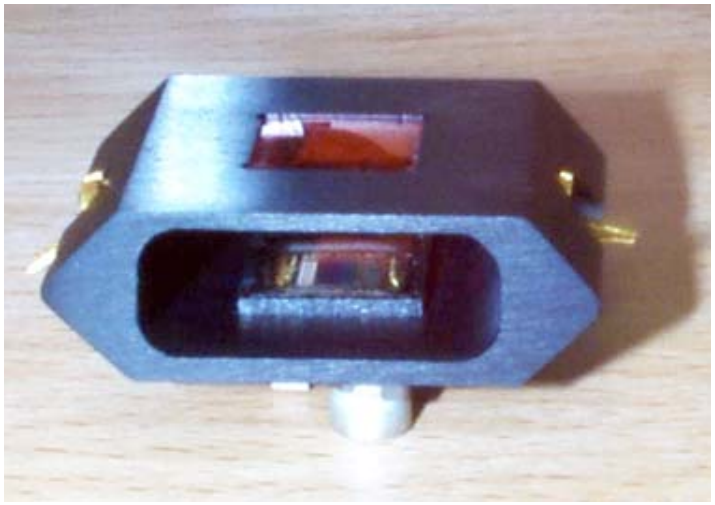
OPGA chip

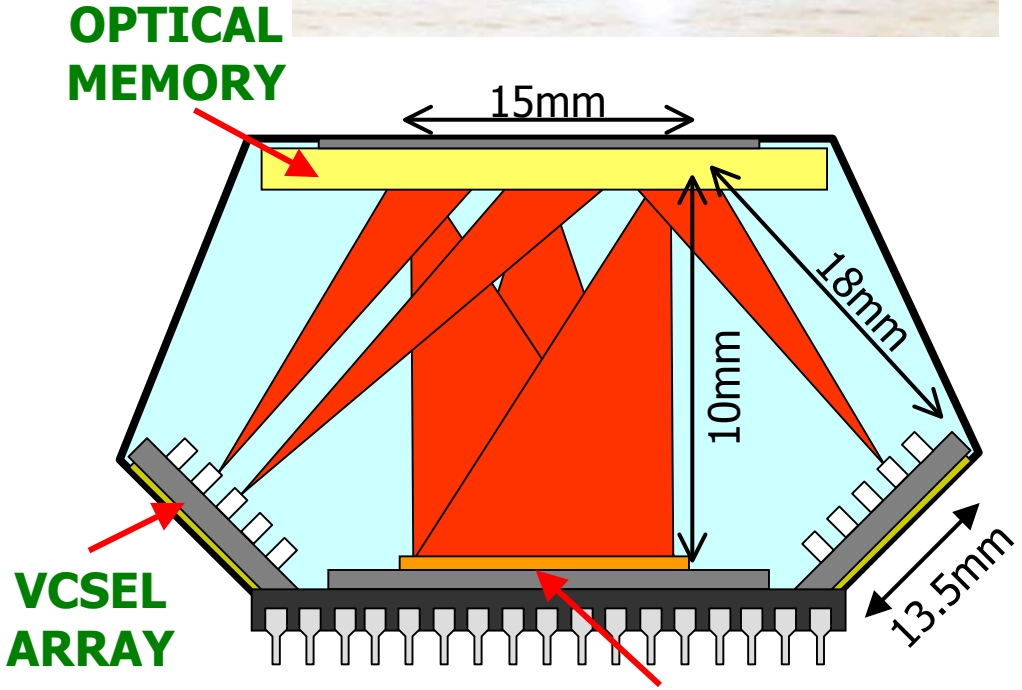


OPGA Module



Optical Memory Silicon Circuit Interface





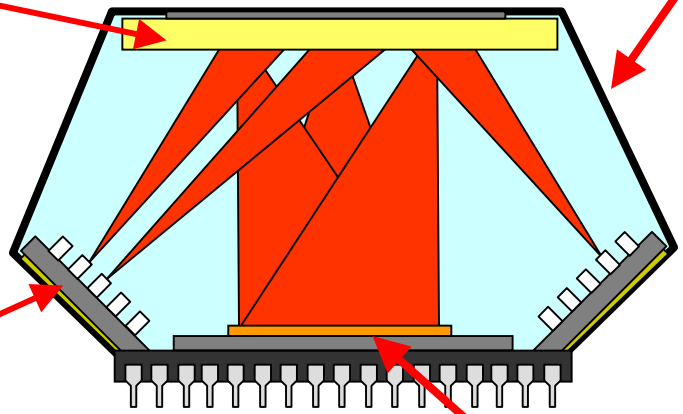
OPGA Elements

PACKAGING

HOLOPLEX
UCSD

HOLOGRAM

CALTECH
APRILIS



ADDRESSING DEVICE

Red VCSELs: HONEYWELL

MEMS

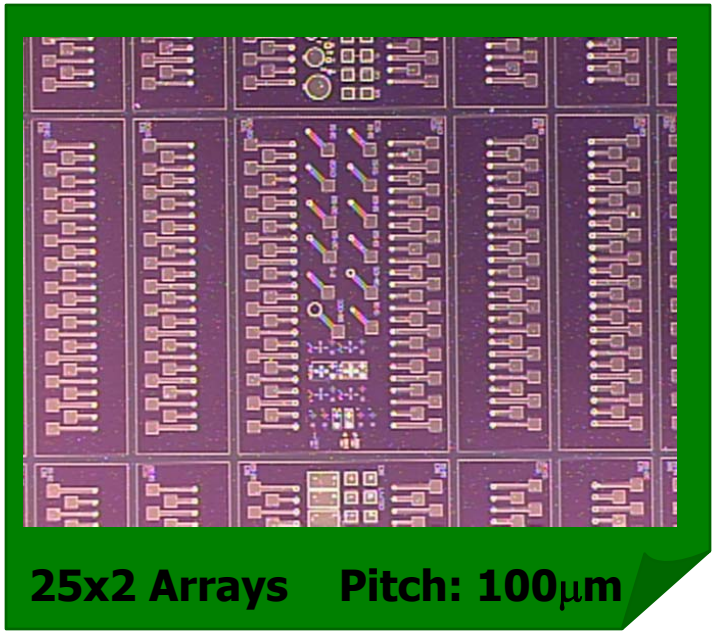
LOGIC + DETECTORS

PHOTOBIT

ALGORITHMS CALTECH

25x2 VCSEL Arrays

Honeywell

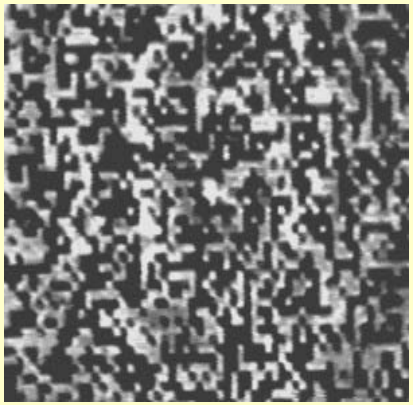


25x2 Arrays Pitch: 100μm

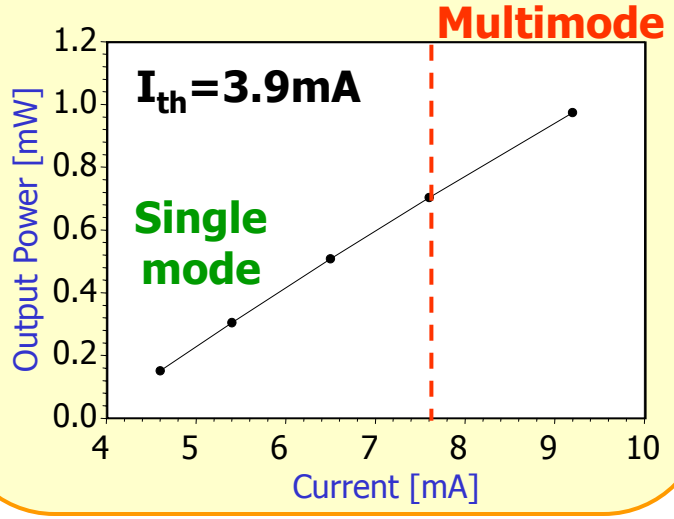
Design specifications: **Status:**

- Array dimensions: 25x2	✓
- Device pitch: 100mm	✓
- Wavelength: 680nm nominal	✓
uniformity: <0.05%	✗
die-to-die consistency	✓
- Power: >0.5mW single-mode	?
- Power uniformity: +/-5%	?
- Beam divergence: >8° within +/-10%	✓
- Packaging (with multiplexors):TO5(ϕ1/4")	

VCSEL Holography



Power: >0.5mW single-mode



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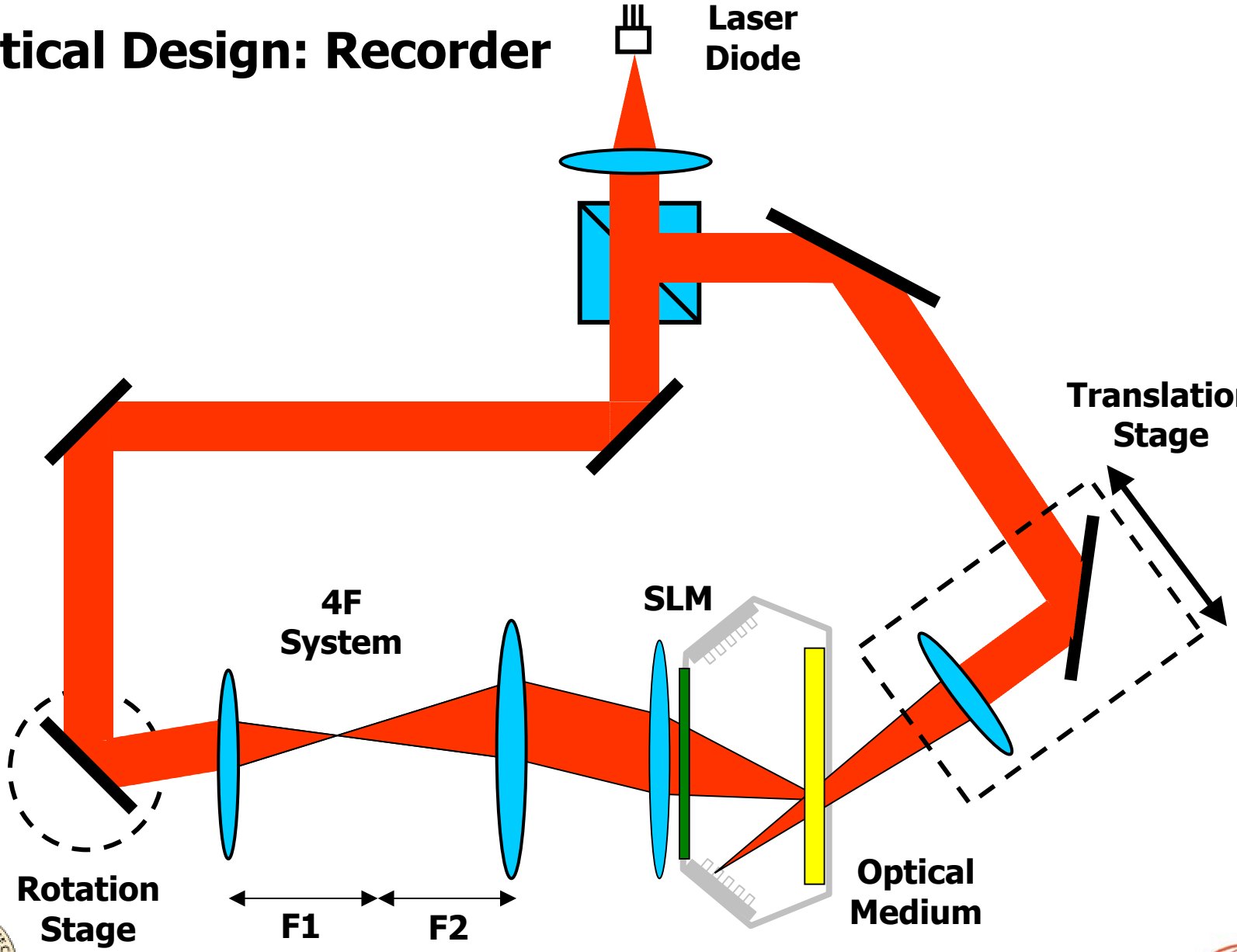
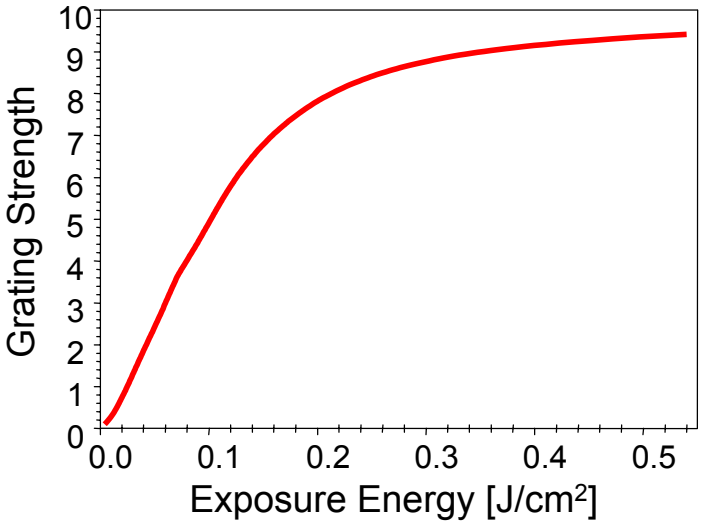
Optical Design: Recorder



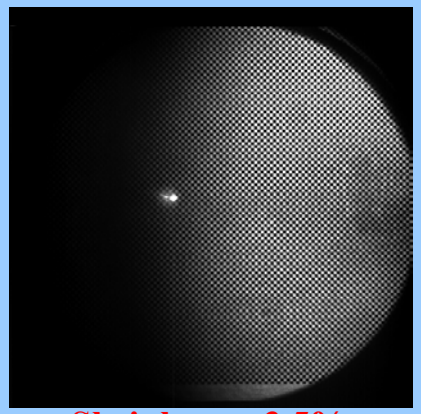
Aprilis Material

M# measurement



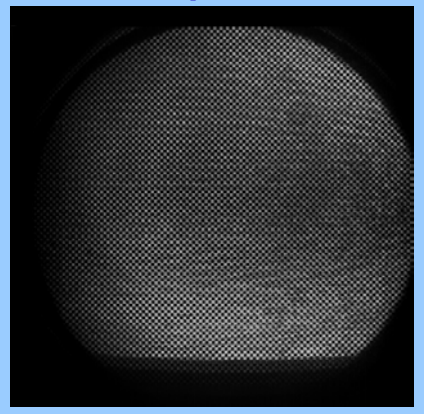
Material Shrinkage

DuPont



Shrinkage ~3.5%
(mostly longitudinal)

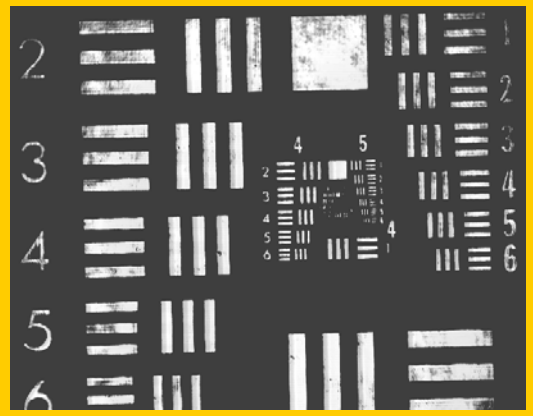
Aprilis



Shrinkage ~0.05%
(mostly lateral)

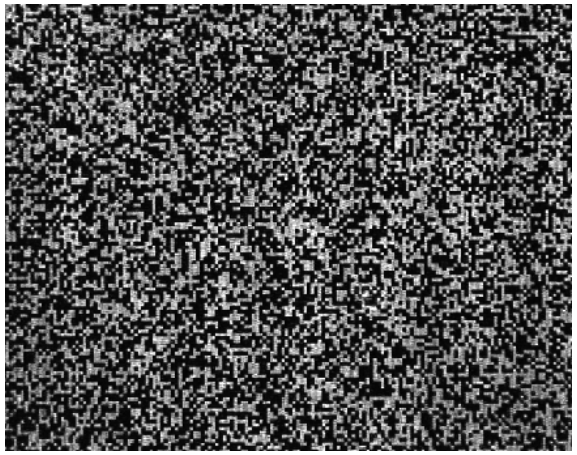
Optical quality:	Excellent (λ/10 over 2mm)
Low scattering:	$<10^{-5}$ srad^{-1}
Thickness:	~500μm
M/#:	10 (5 with images)
Sensitivity:	1mJ/cm^2 (1% Efficiency)
	300mJ/ cm^2 (saturation)
Deformation:	Shrinkage <0.05%
MTF:	Good (0.2 – 10um)
Uniformity:	Good
Consistency:	better than DuPont

Image Quality



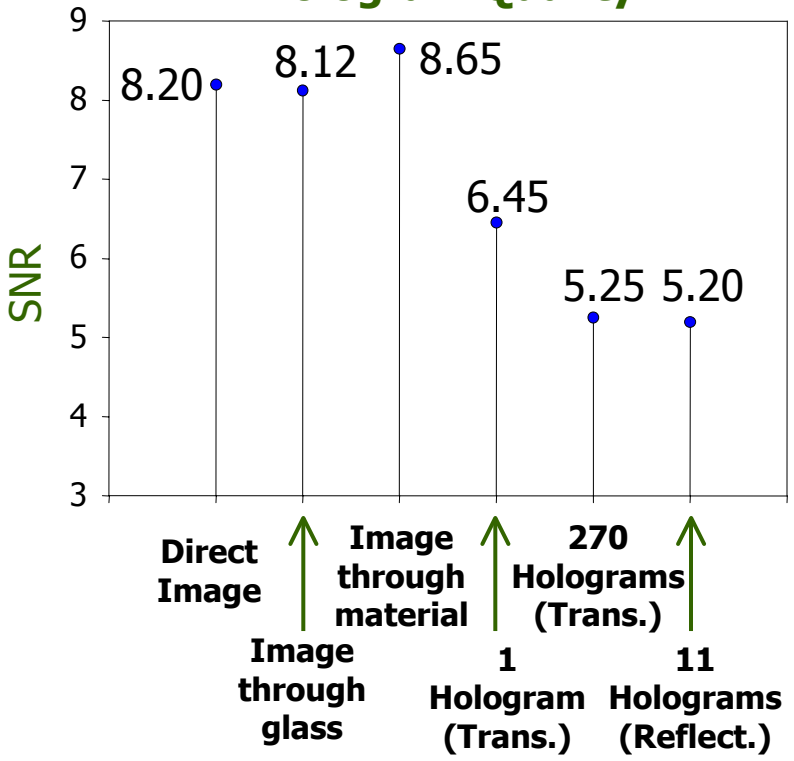
Phase-conjugate readout

Holographic Storage

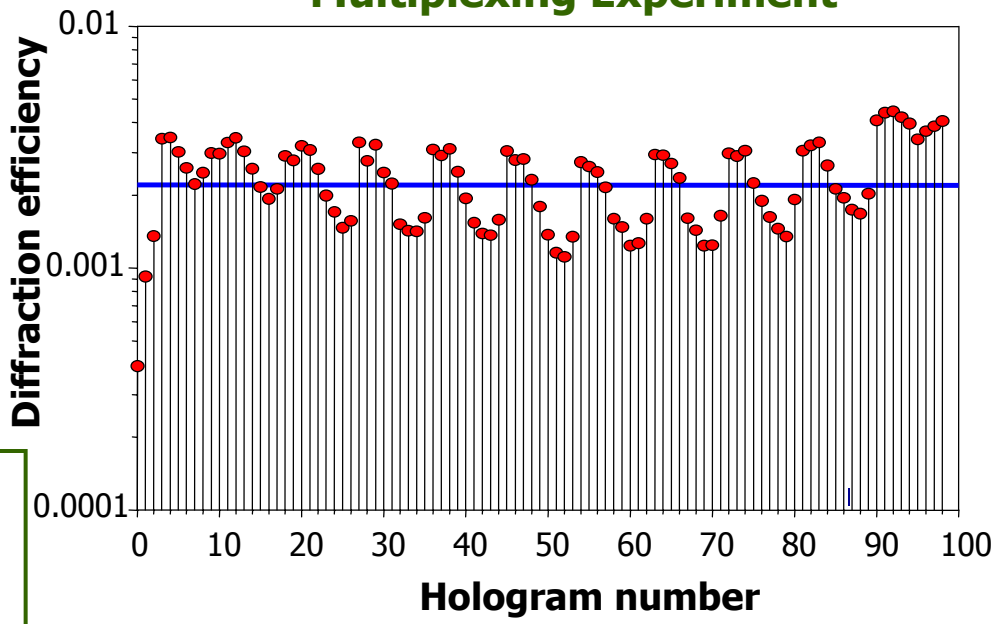


Random-pixel Holographic Datapage

Hologram Quality



Multiplexing Experiment



Average $\eta = 2.38 \times 10^{-3}$

M/# = 4.83

BER= 2.4×10^{-8}

Reconfiguration time: 20μsec

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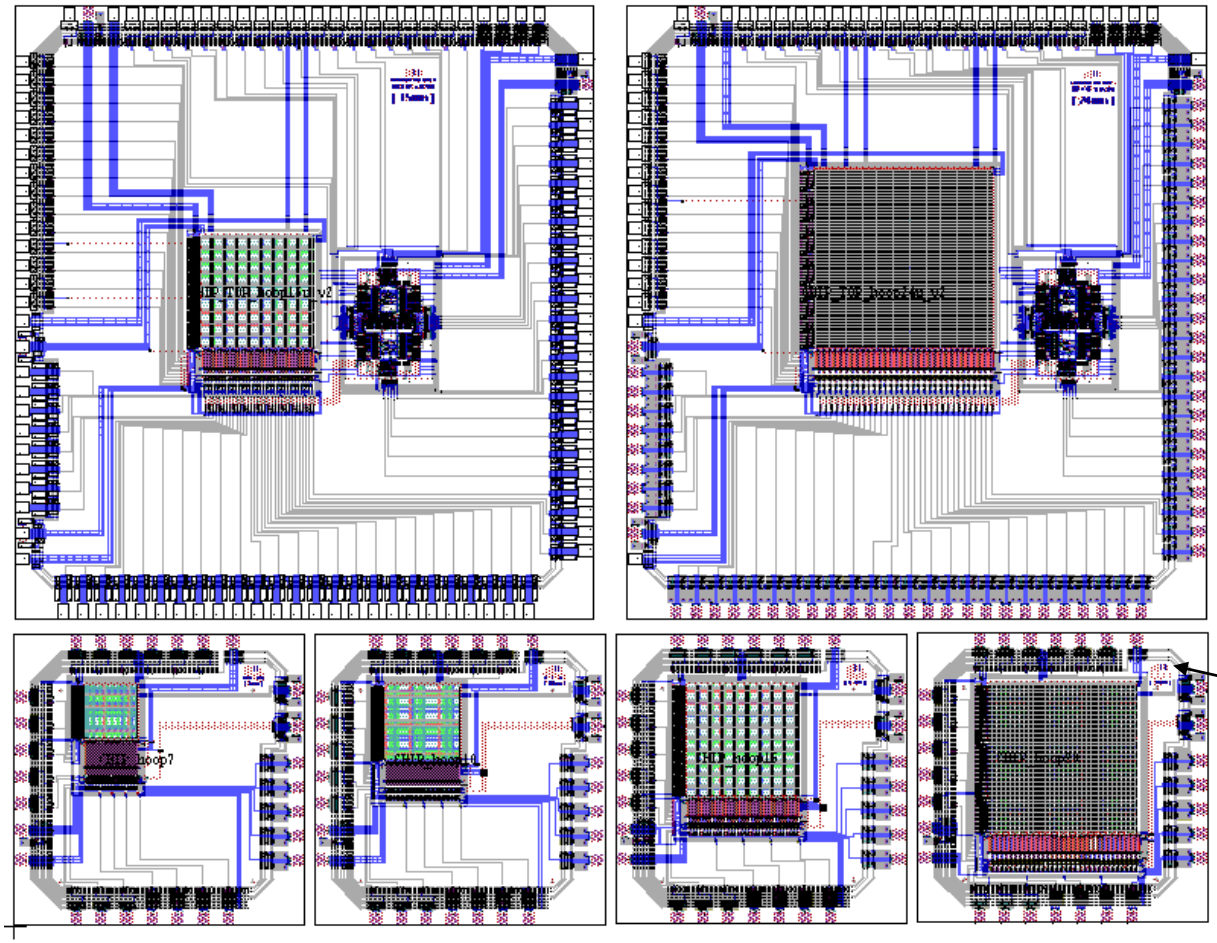
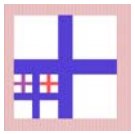
2nd-generation APS chips: tapeout



- FULL OPGA CHIPS
  - 5.01mm X 5.30mm
  - 15um, and 24um pixels
  - 103 PADS
  - Down-left corner aligned
- TEST APS CHIPS
  - 2.53mm X 2.52mm
  - 7um,10um,15um,20um pixels
  - 14 PADS
  - Up-left corner aligned
  - 4 alignment marks (1.6mm apart)



PHOTOBIT-HOLOPLEX
HOOP-v.0100
[15um]

(Alignment Marks)

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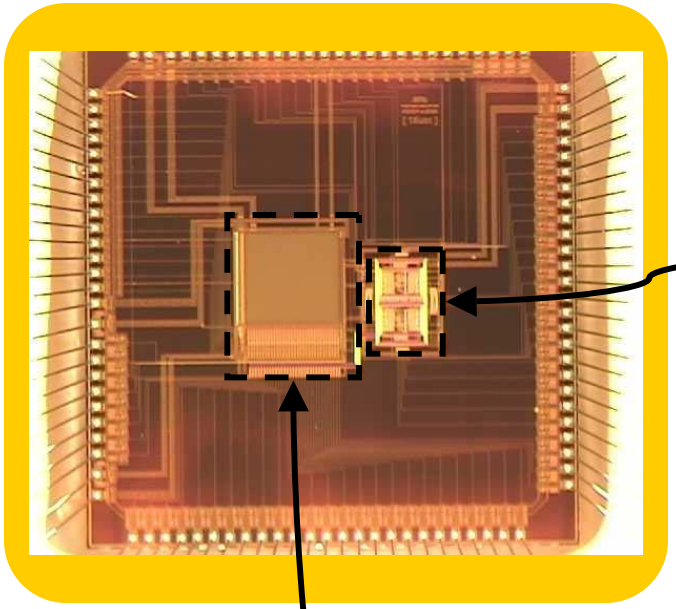
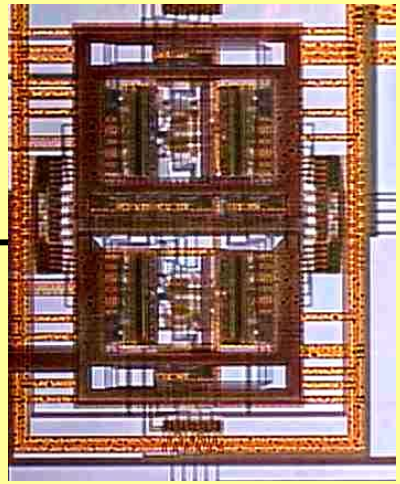
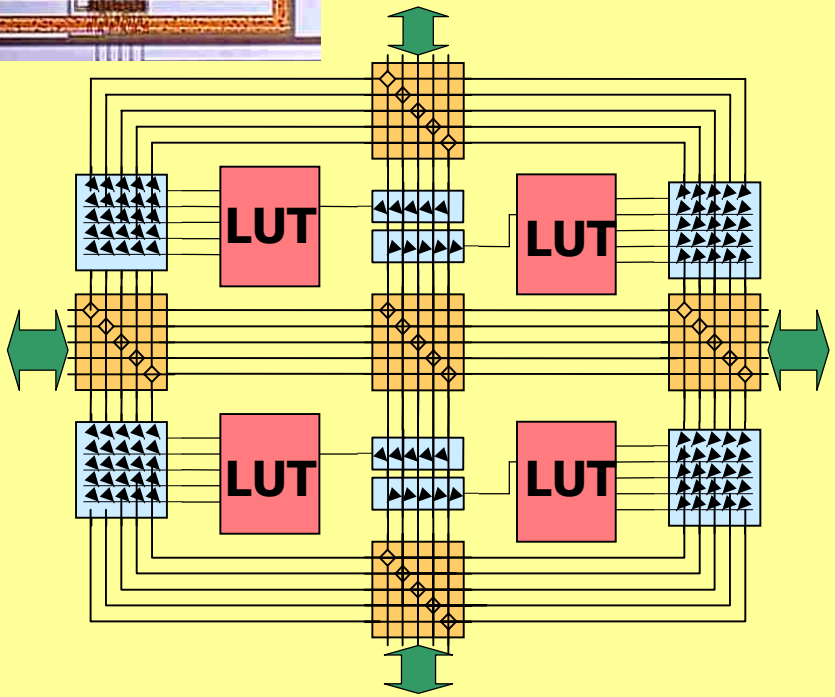
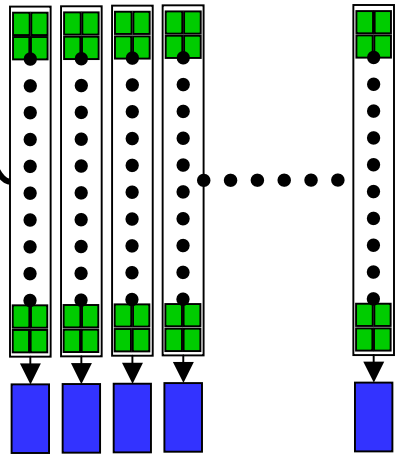
Full OPGA Chip





Customizable logic





64x32 APS Array

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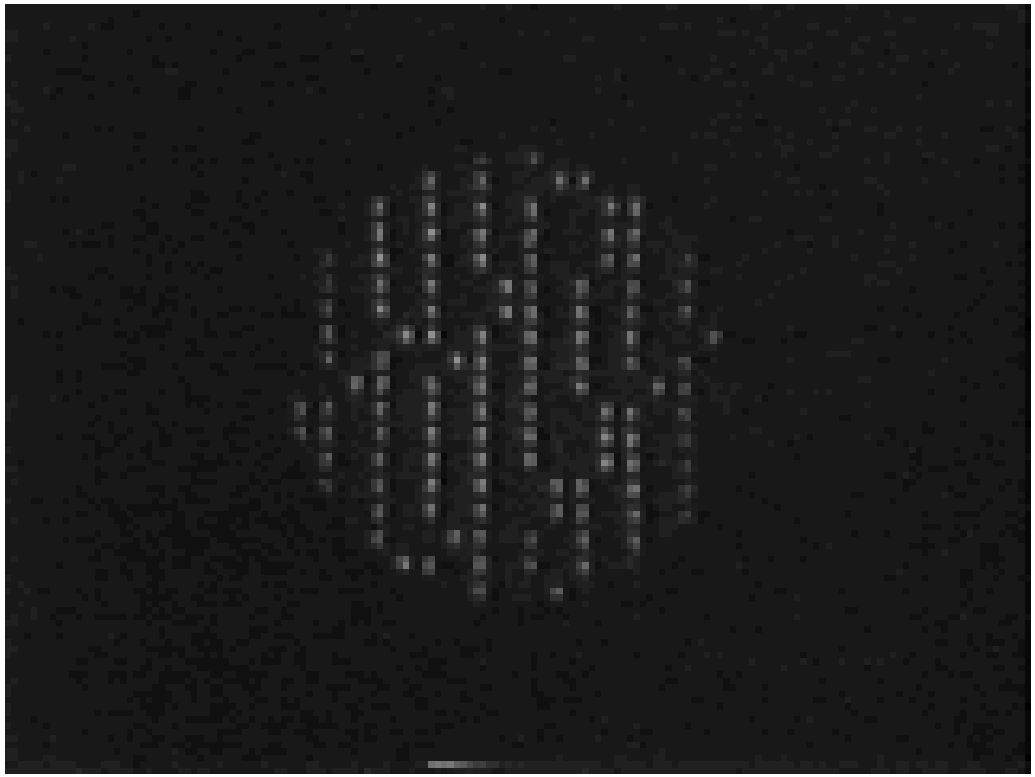
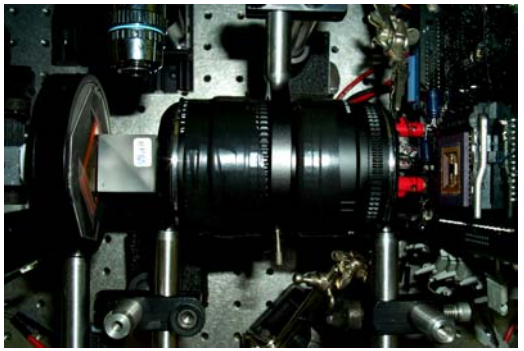
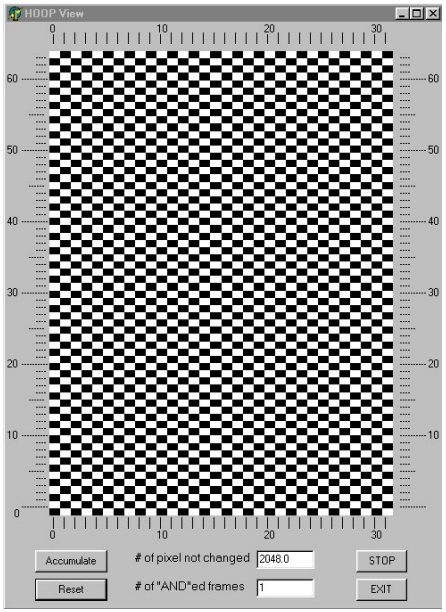
Optical Interface

Experimental Setup



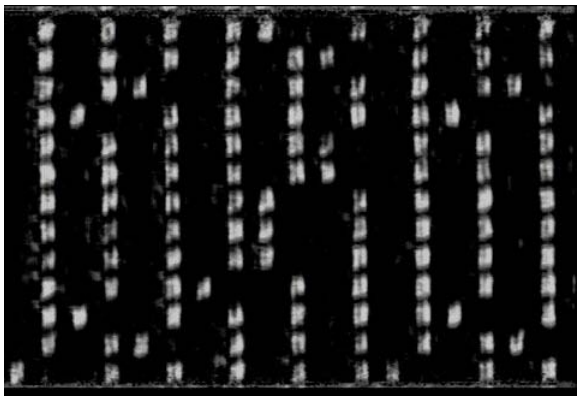




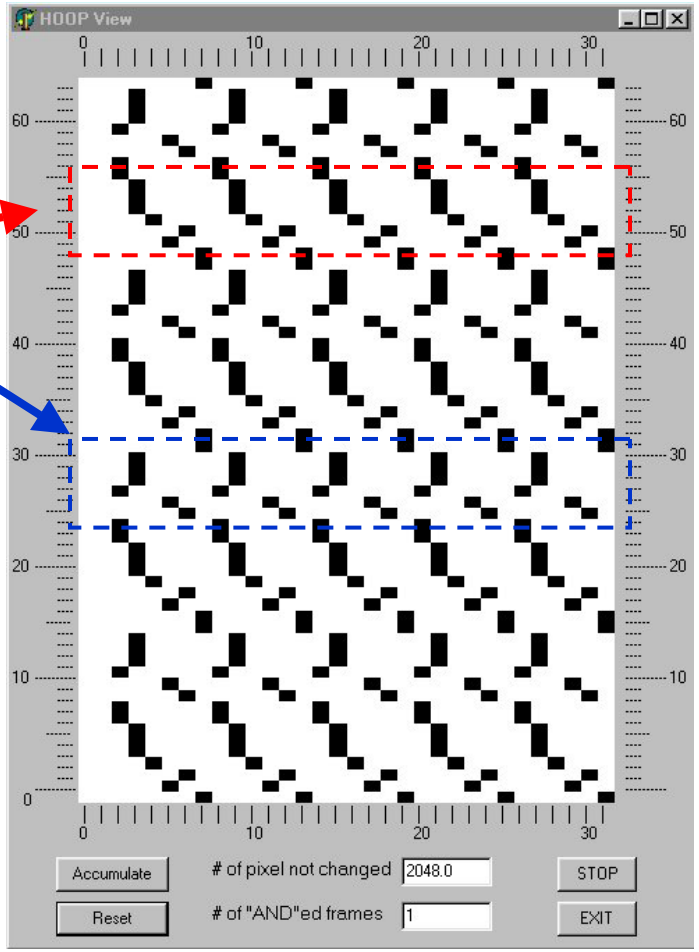
APS Digitized Output

Holographic Programming

Hologram 1

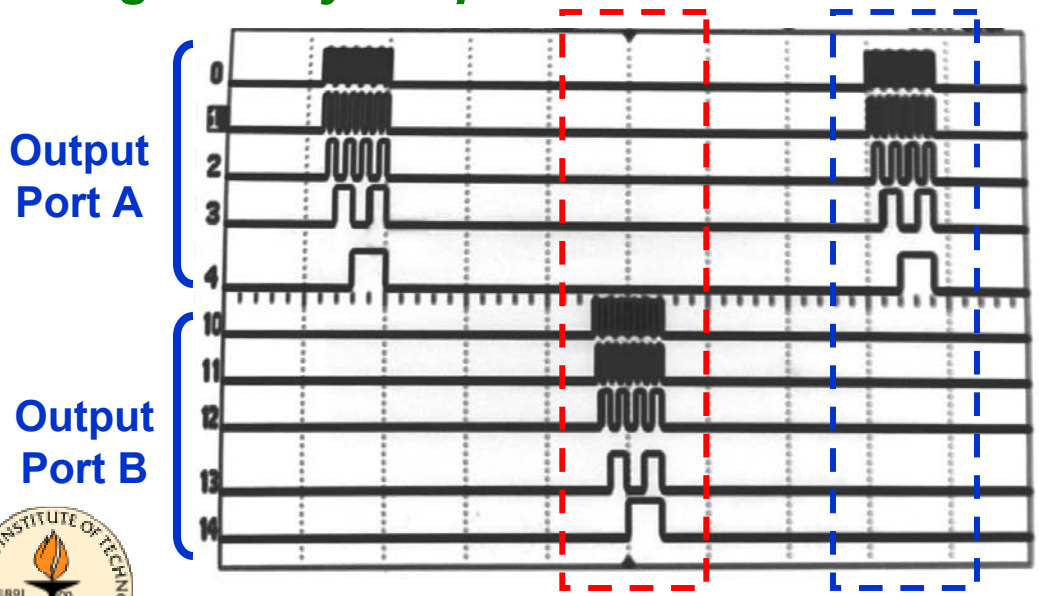


APS Digitized Output



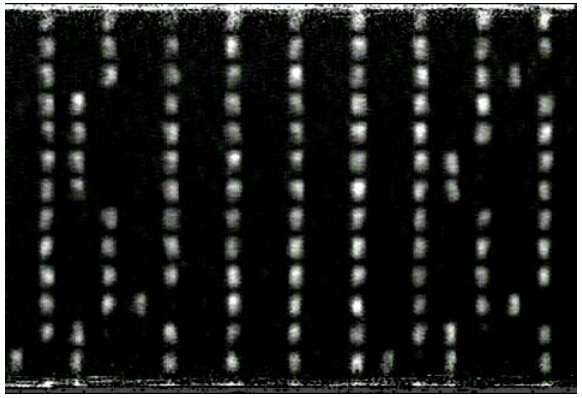
Optical Configuration # 2

Logic Array Output

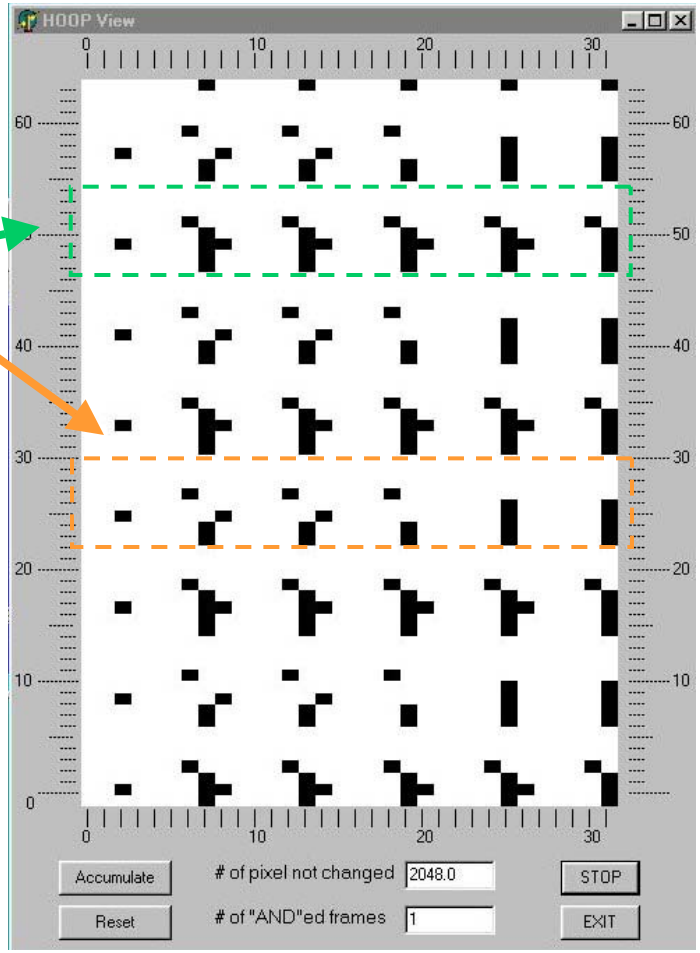


Holographic Programming

Hologram 2

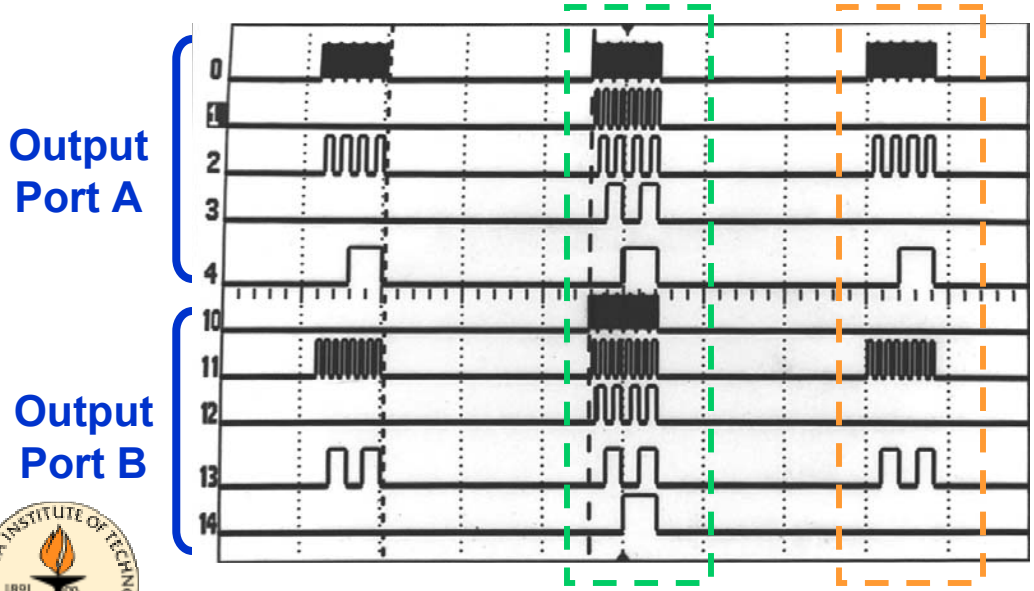


APS Digitized Output



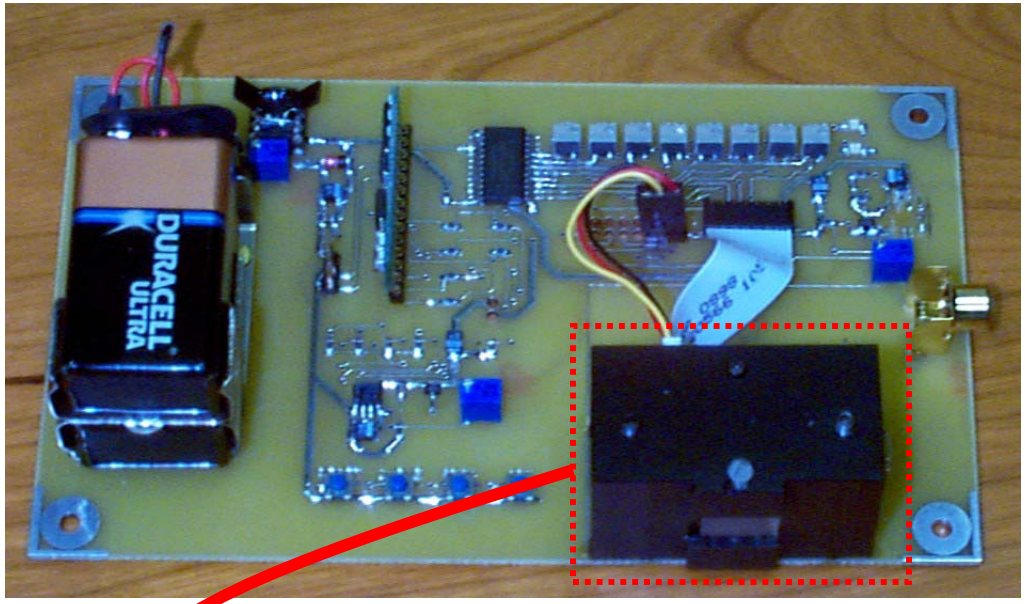
Optical Configuration # 1

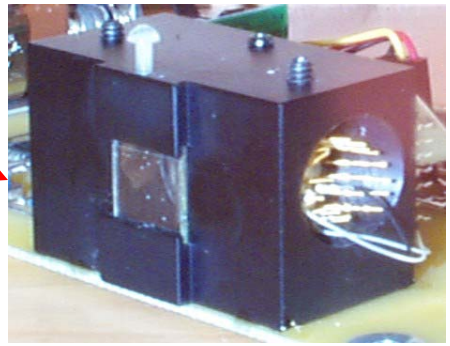
Logic Array Output



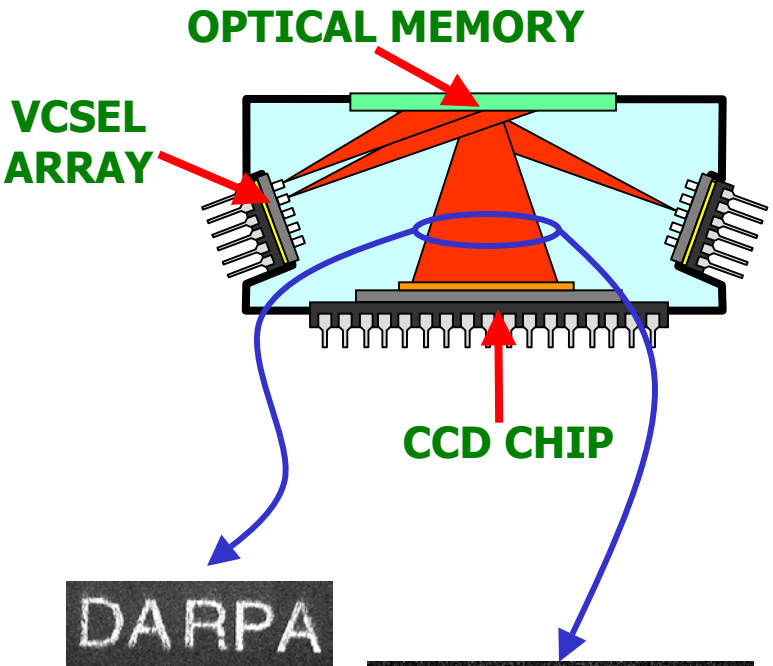
Module Packaging

OPGA Driver Board

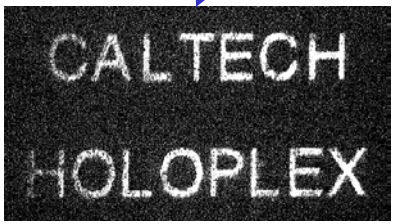




OPGA Module



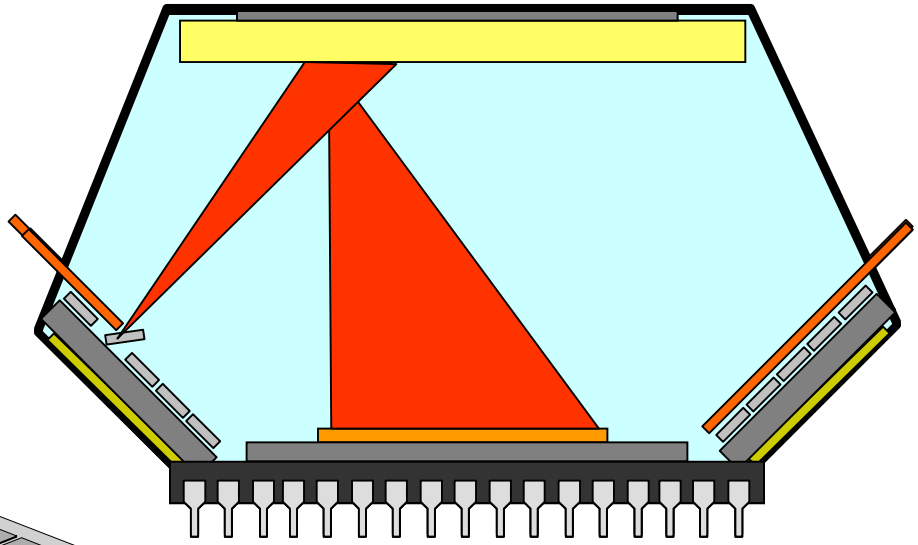
Hologram #1

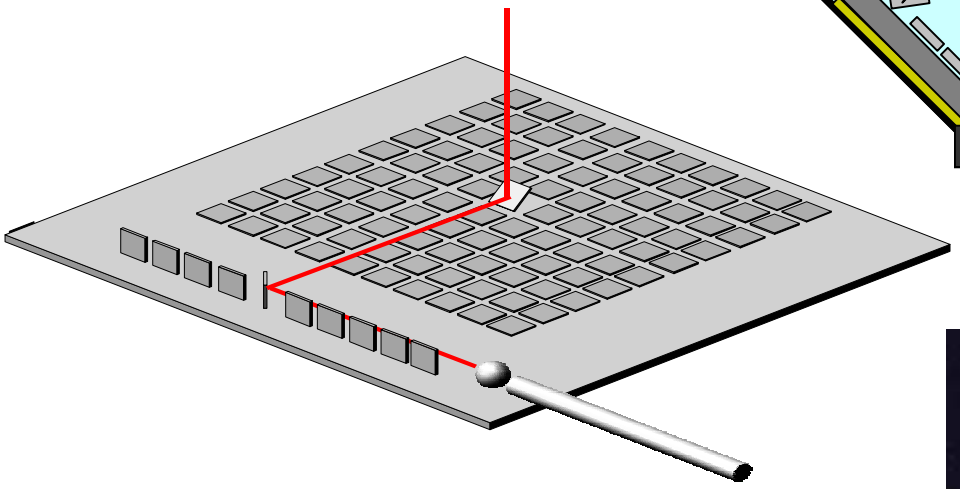


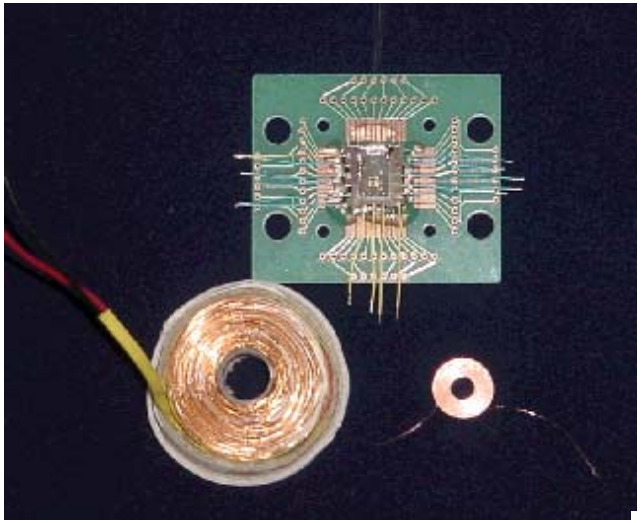
Hologram #2

Shift-multiplexed Holograms

MEMS addressing

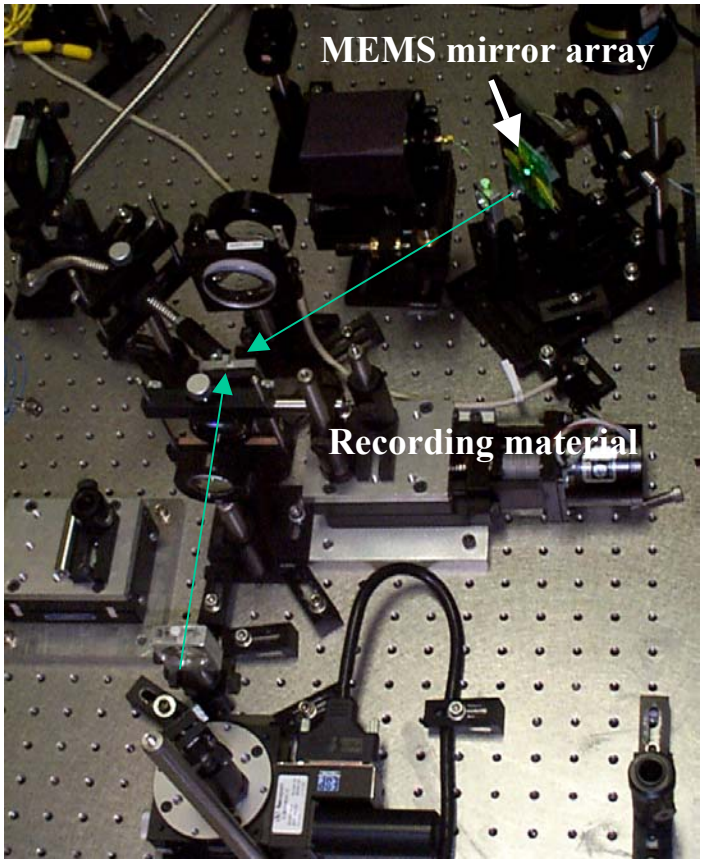


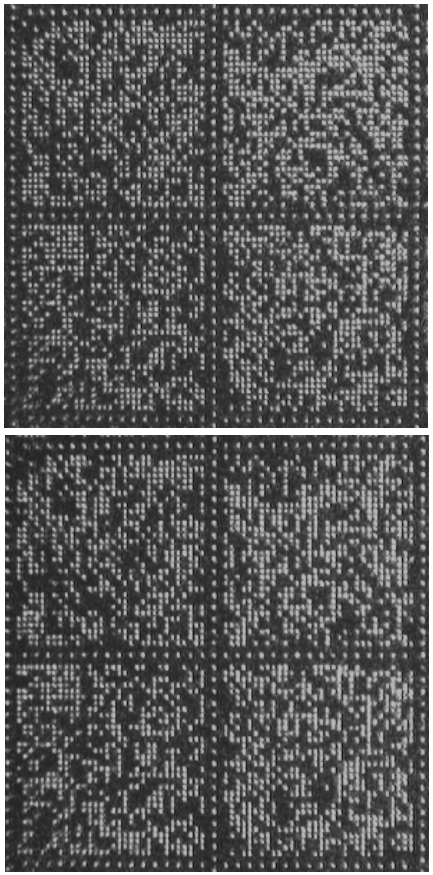




- 4x10 mirror array
- Mirror dimensions:
  100μm x 100μm
- NA/0.2 output

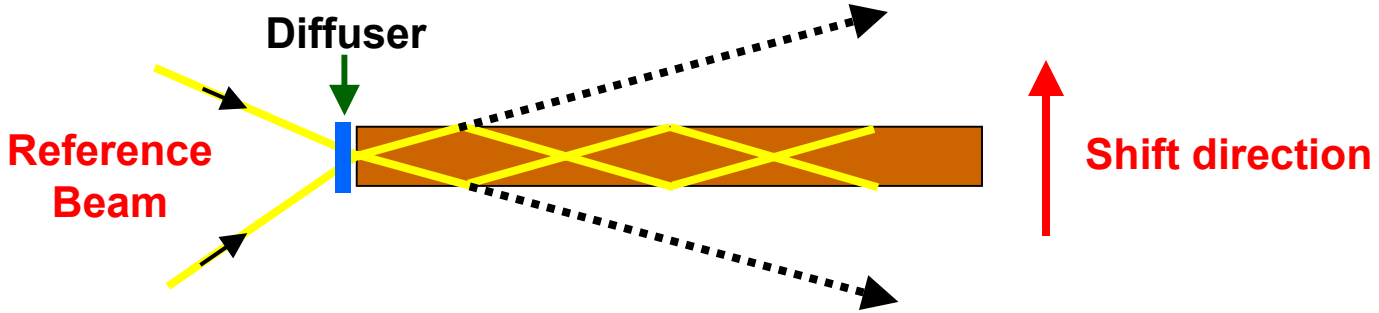
Experiment setup and results

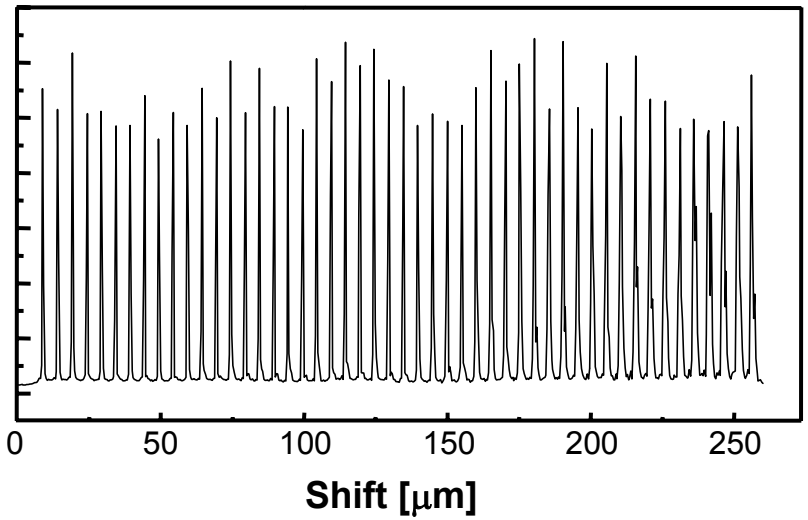


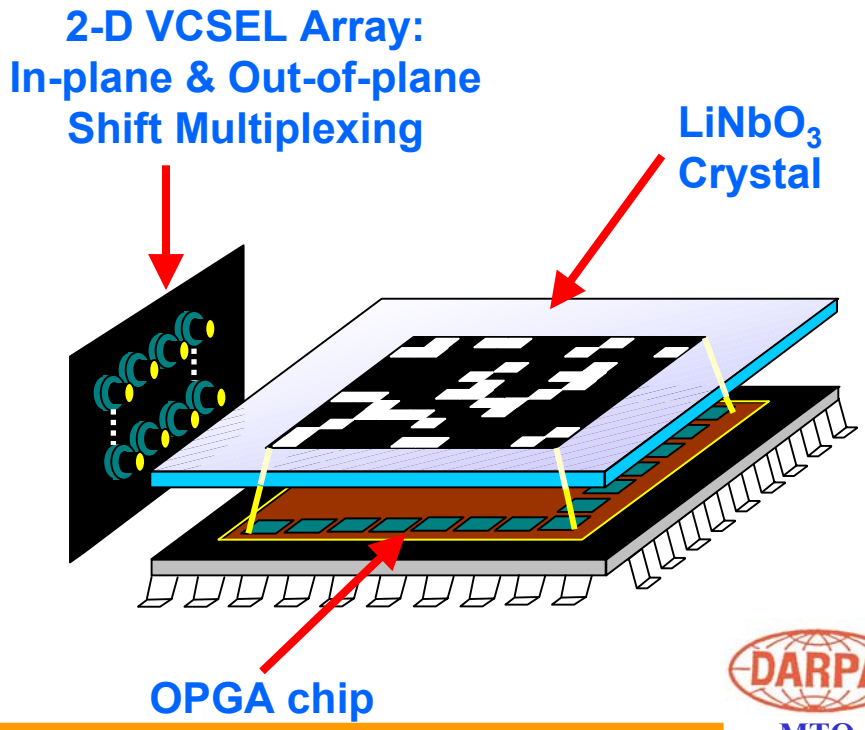


MEMS throughput efficiency: 30%

Compact Packaging: Multiplexing







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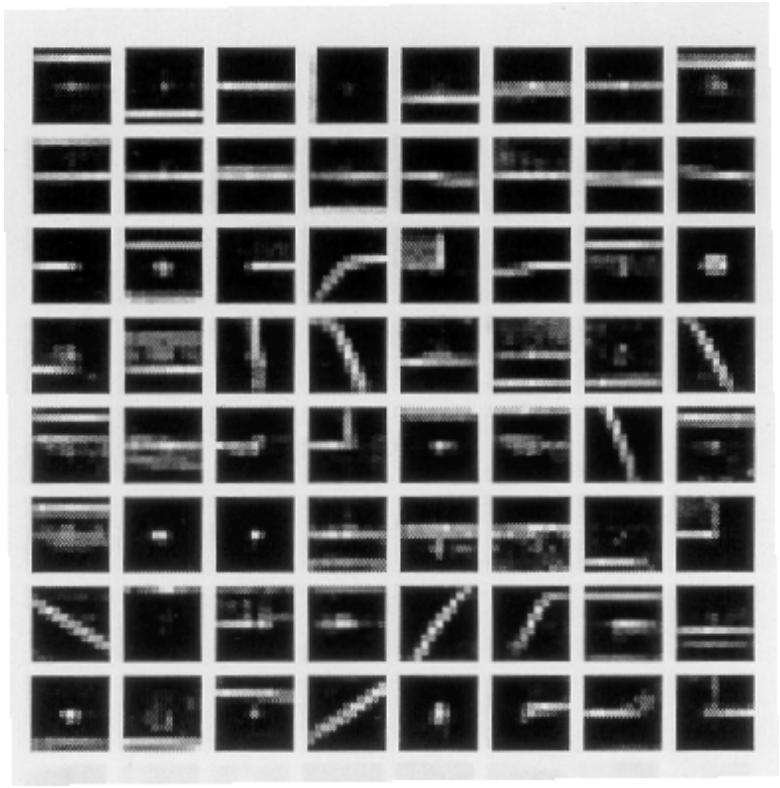
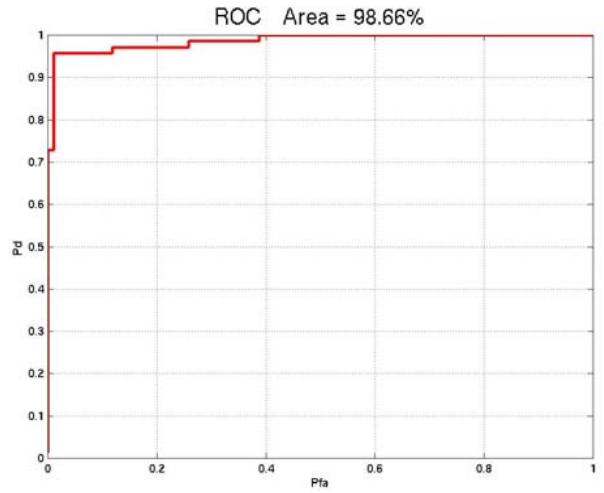
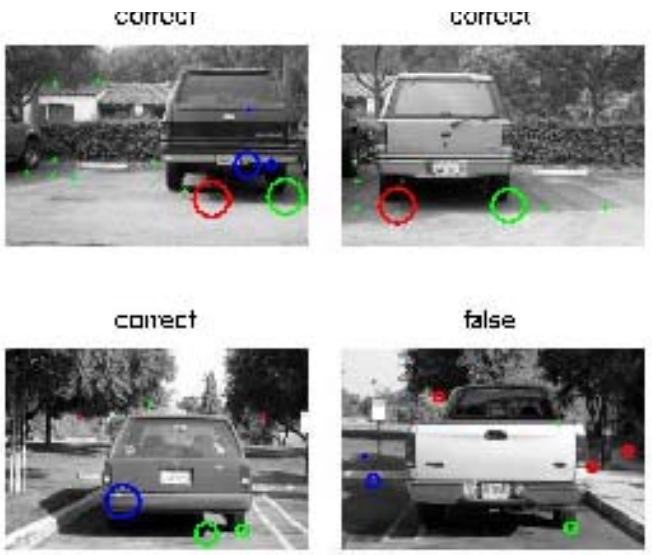
Constellation model

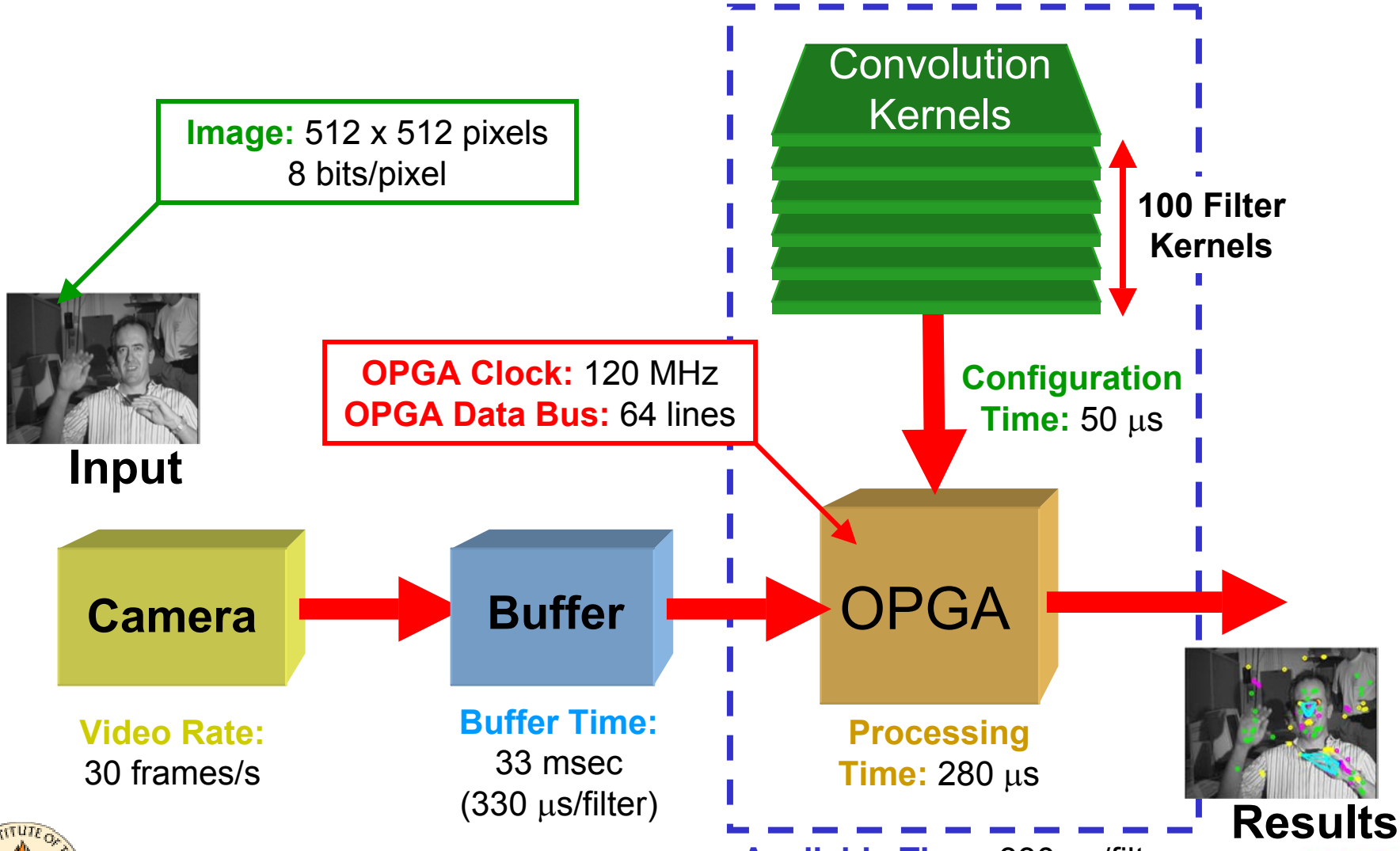




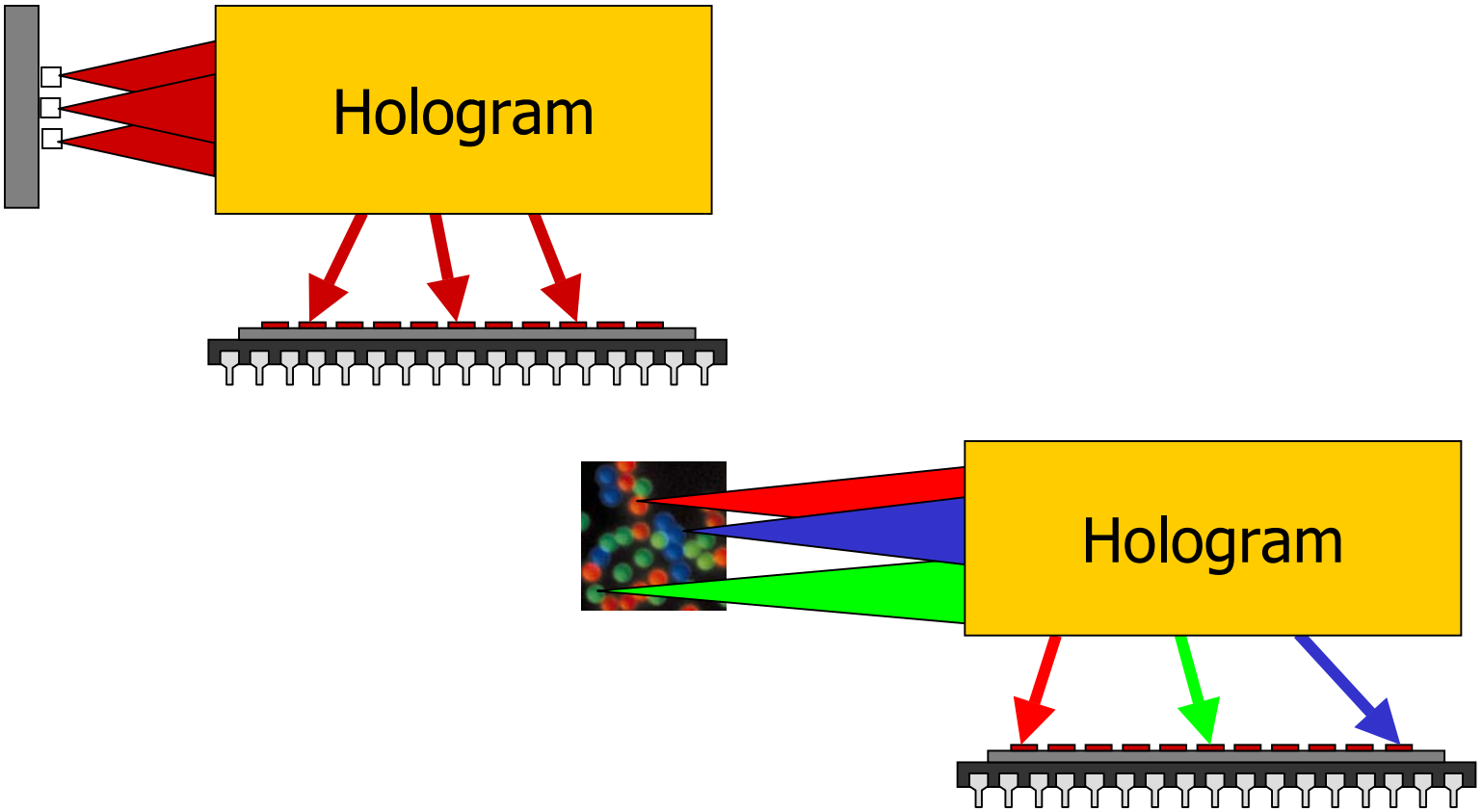


http://www.vision.caltech.edu/html-files/publications.html

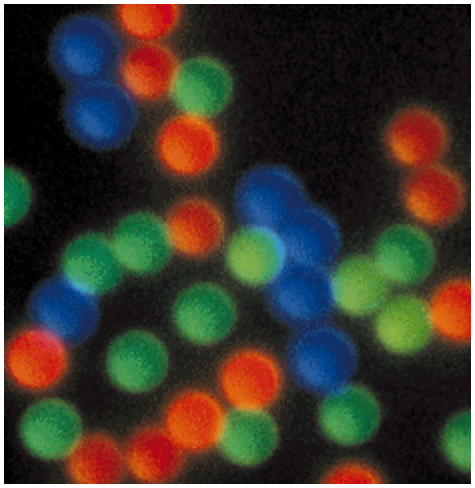
OPGA for Real Time Video Processing



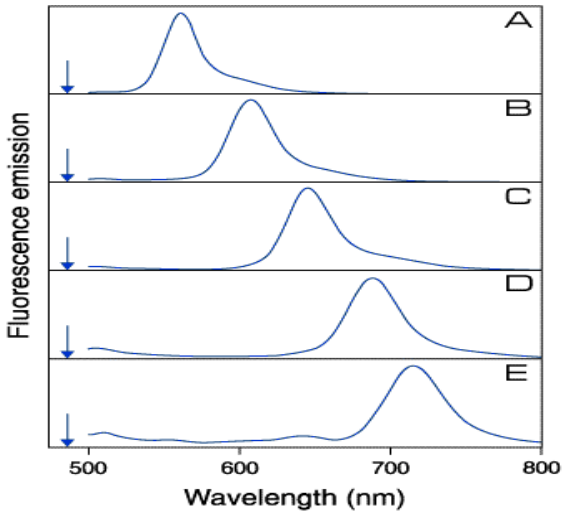
Memories vs. Imaging Elements

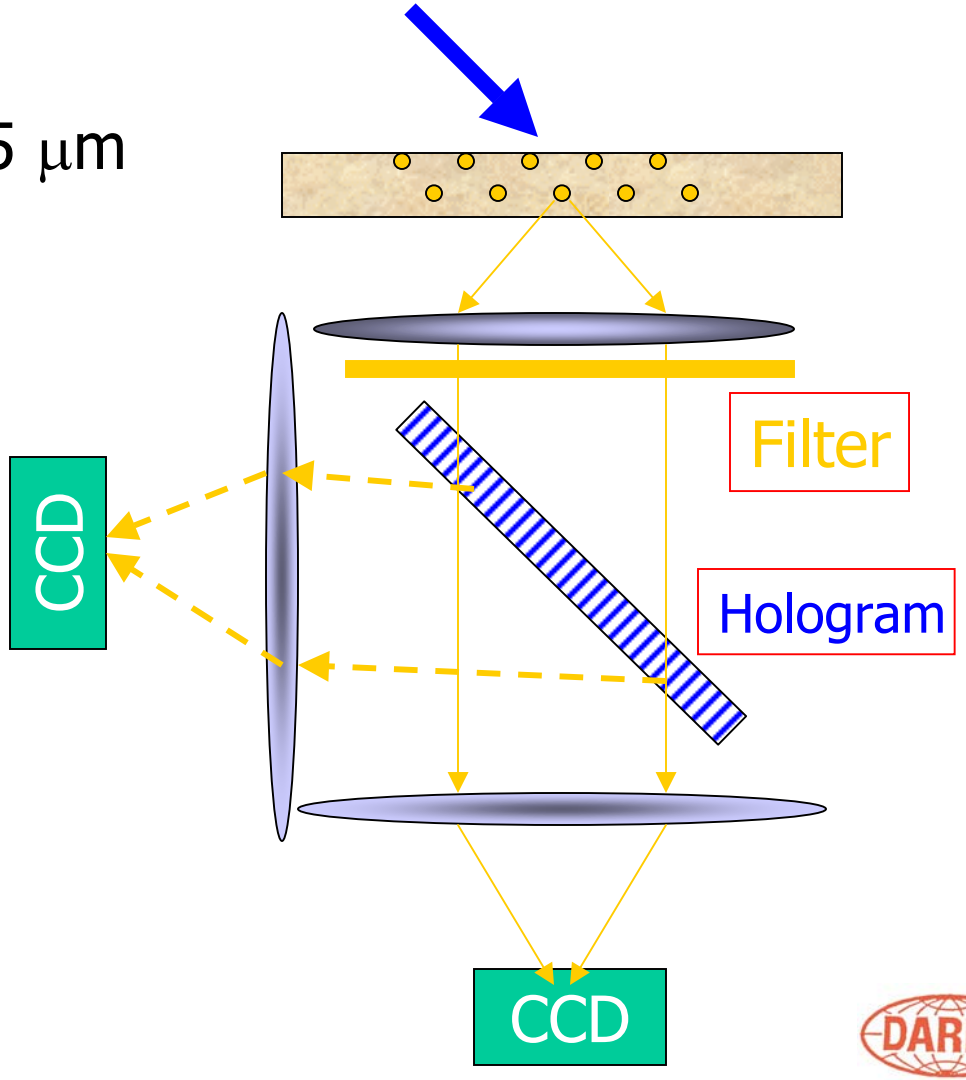


Holographic 4-D Imaging



15 μm



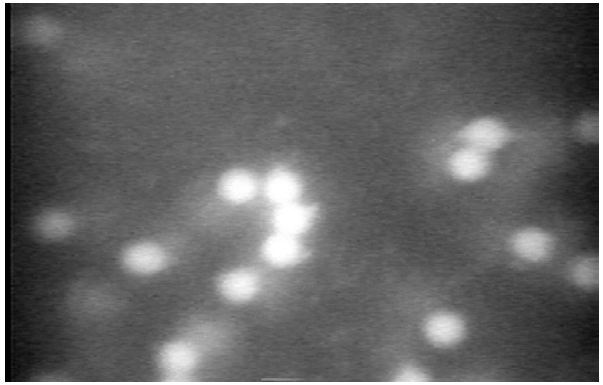


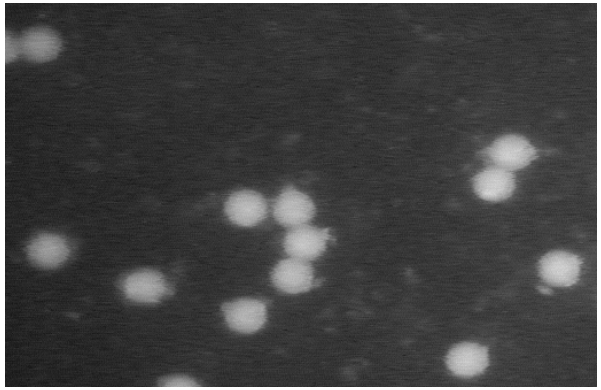
Images of double-layer microspheres

Holographic spectra

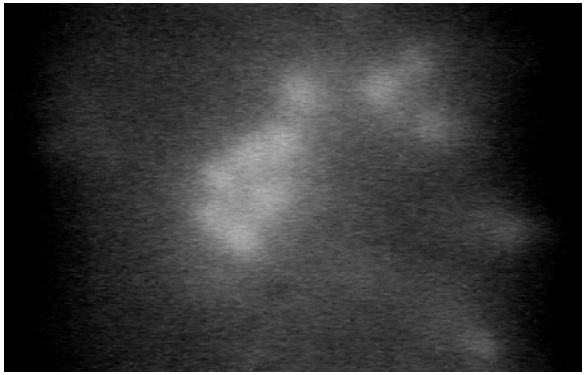
Microscope image

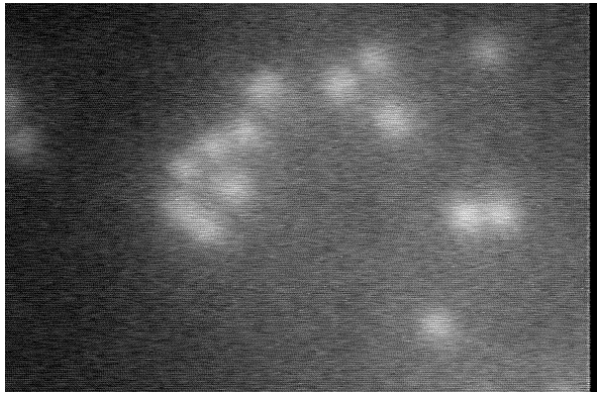
1st layer



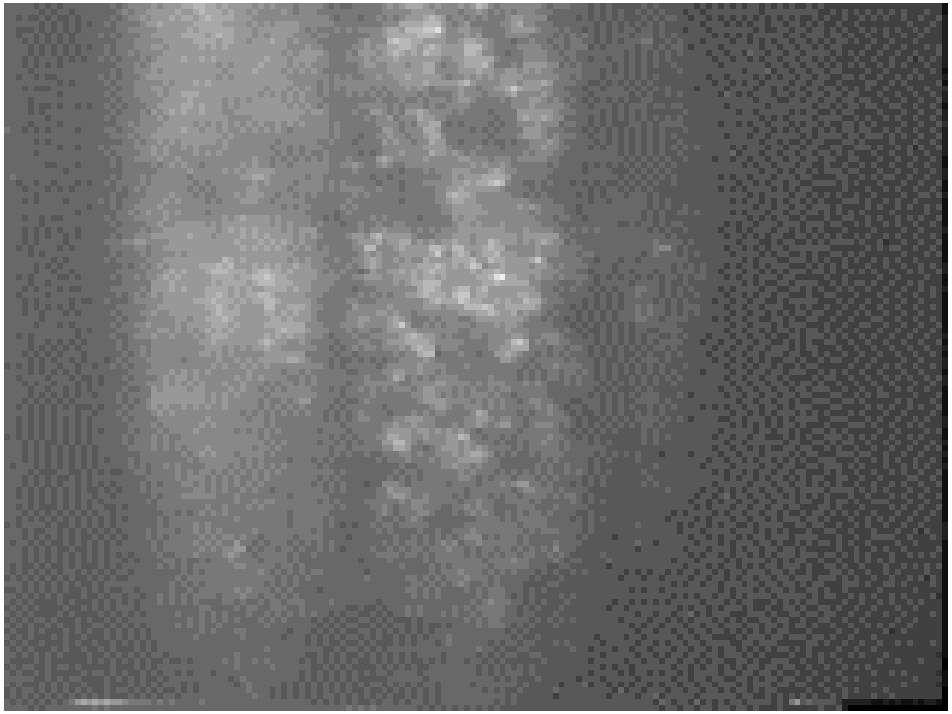


2nd layer





3-layer imaging of fluorescent microspheres in turbulence



y

x-λ

Accomplishments

- **VLSI Chip Design:**
  - Demonstration of optically reconfigurable logic circuits
  - Holographic programming of the OPGA chip
- **Optical Memory:**
  - Material testing/selection completed: Aprilis polymer
  - Mastering and multiplexing in Aprilis films
  - 100 Holographic reconfiguration templates
- **Addressing devices:**
  - Red VCSEL arrays (25x2) packaged and tested
  - Phase-conjugate read-out
  - MEMS array holography
- **Packaging**
  - Demonstration of compact module including VCSELs, Holograms and Silicon
  - Advanced packaging technique demonstrated
- **OPGA Applications:**
  - Image processing; Image database search
  - Prosthetics