Manufacturable SiC Power MOSFETs

Anant Agarwal, Sei-Hyung Ryu and John Palmour

Cree, Inc.

4600 Silicon Drive

Durham, NC 27703.

Nelson Saks

NRL

Funded by DARPA/ONR

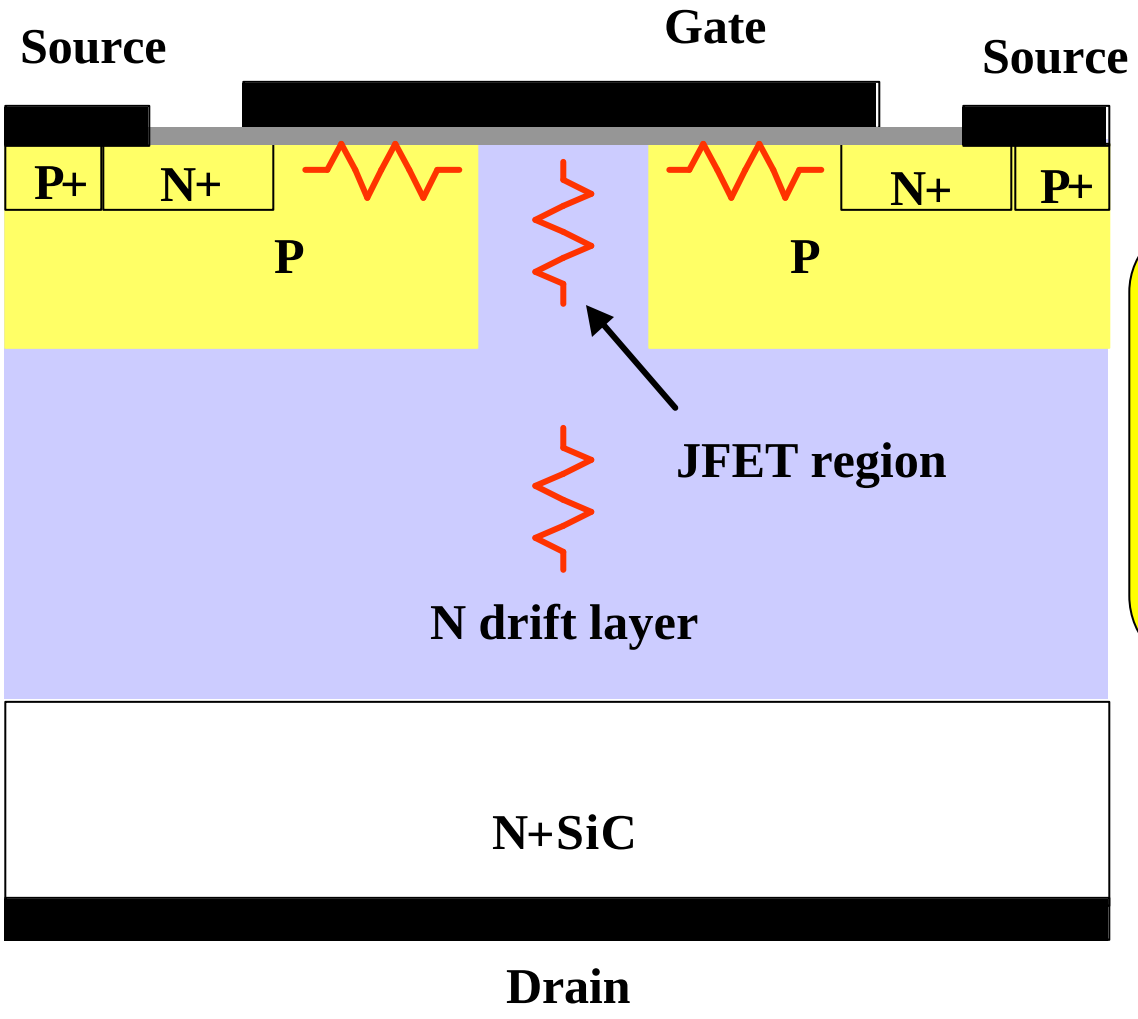
Outline

- Background
- Device design
- 2D simulation
- Device layout
- Results
- Summary

Which Structure ?

- **UMOSFET**
- **Lateral DMOSFET**
- **DIMOSFET**

The DMOSFET Structure



Design Issues

- N drift layer doping/thickness
- Spacing between two p-wells
- Maximum gate oxide field under blocking condition
- On-Resistance

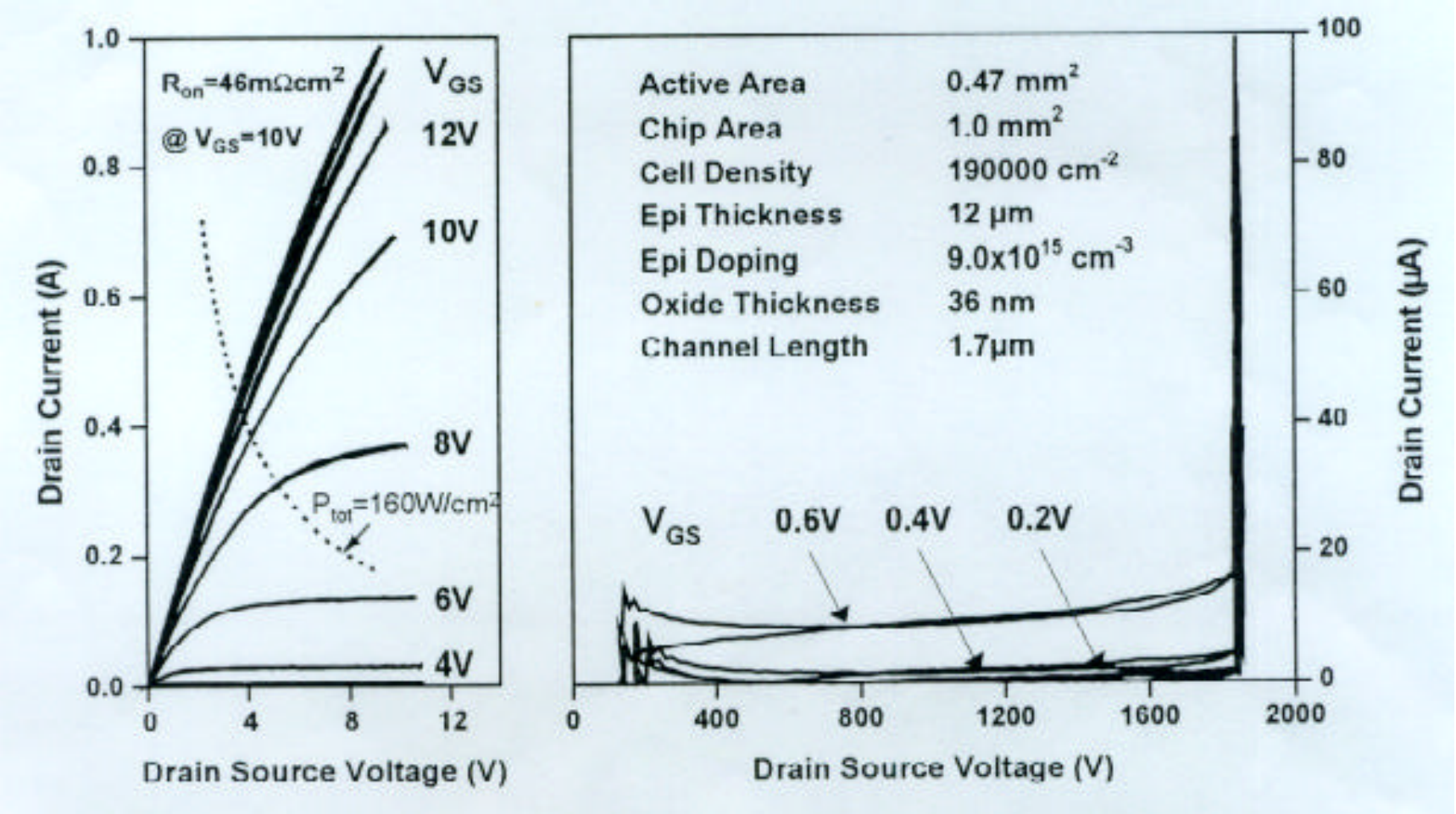
Critical Issues

- **Achievement of μ_{ne} > 25 $cm^2/V \cdot s$ with <u>implanted P-Wells</u> and <u>Annealed Contacts</u>**

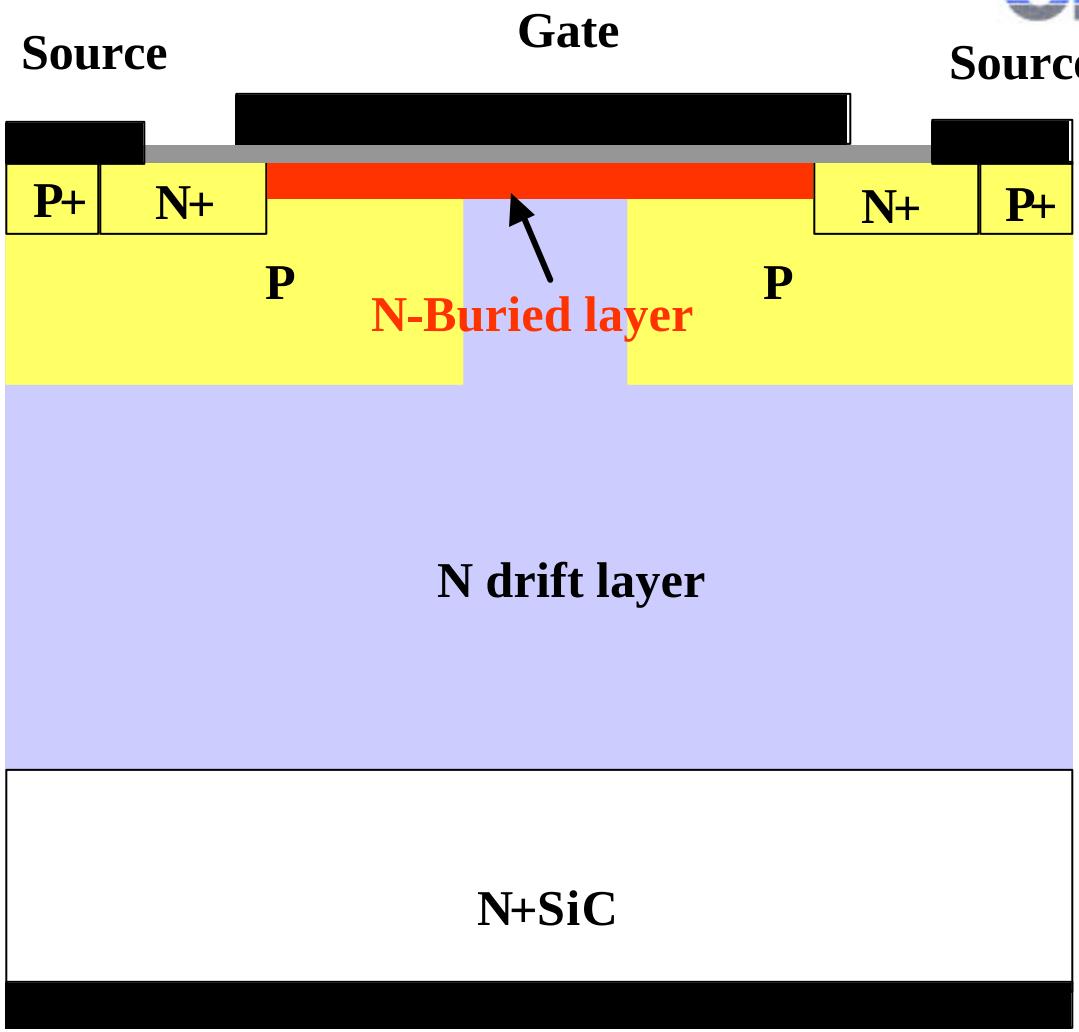
- **Achievement of 2000 V and 50 A <u>simultaneously</u> in a 5.5 mm x 5.5 mm chip**

Background

Siemens 6H-SiC Power MOSFET, 1mm x 1mm

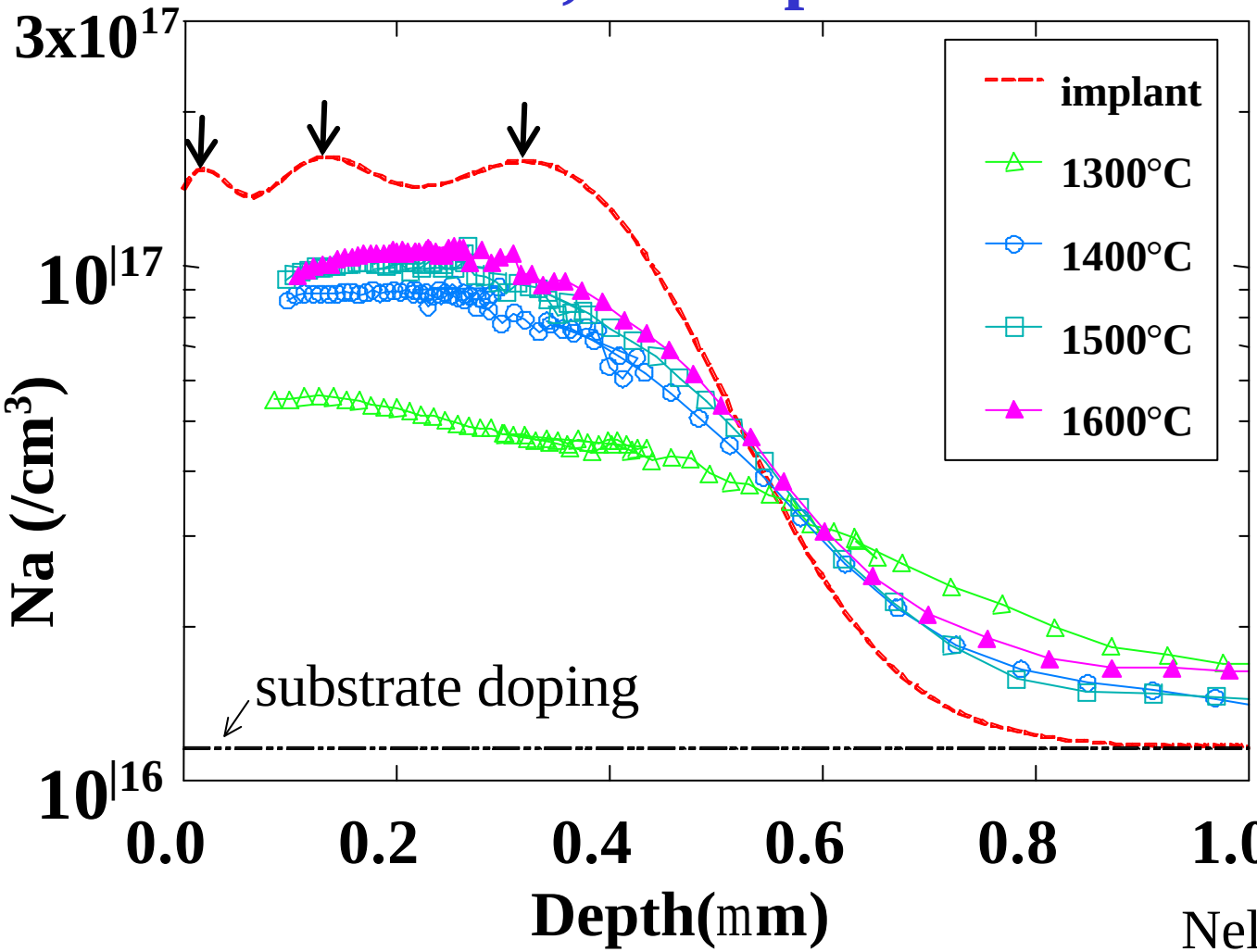


Buried Channel Device



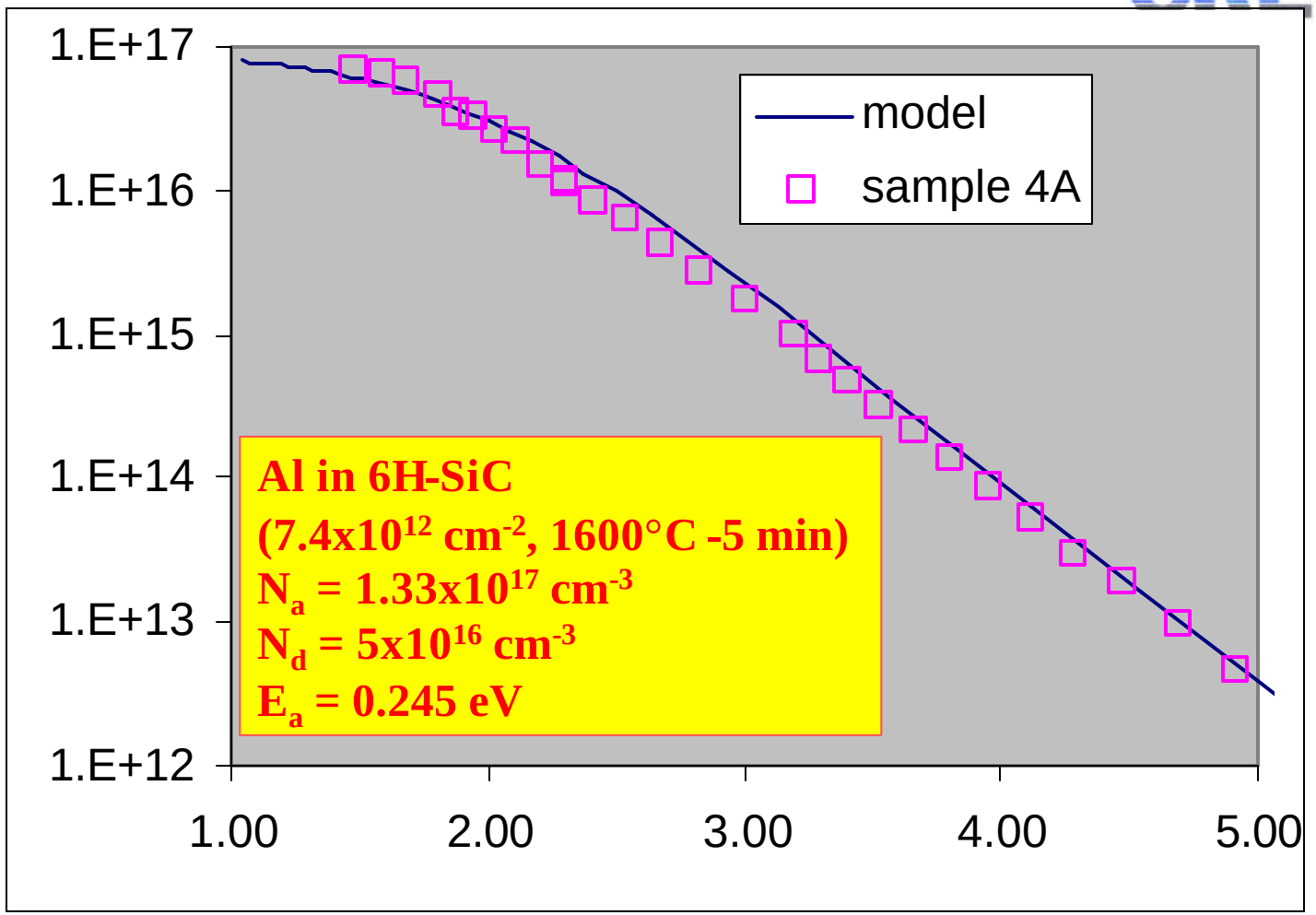
Implant Activation CV Analysis

6H-SiC, Al Implanted



Nelson Saks

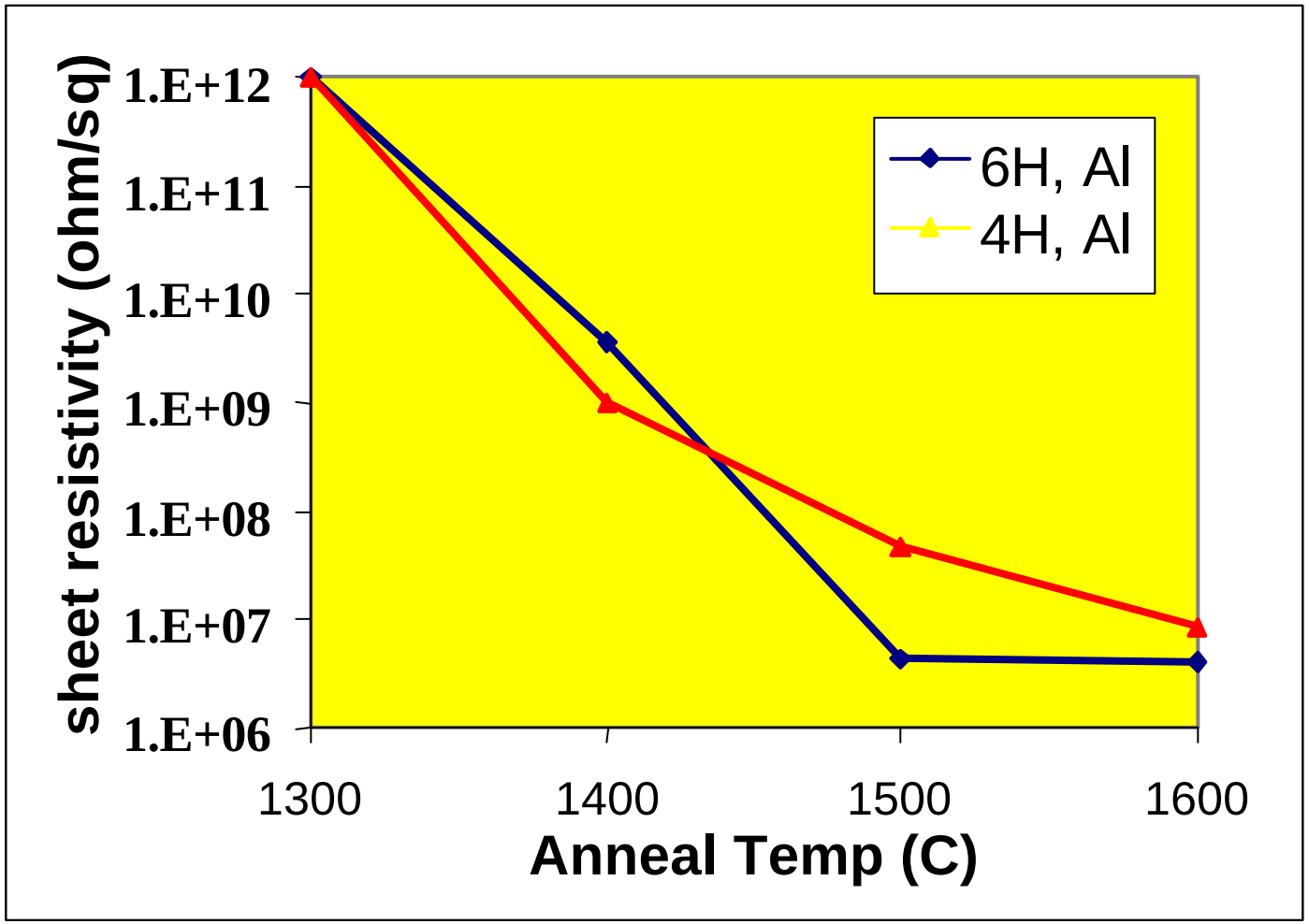
Implant Activation
High Temp. Hall Data



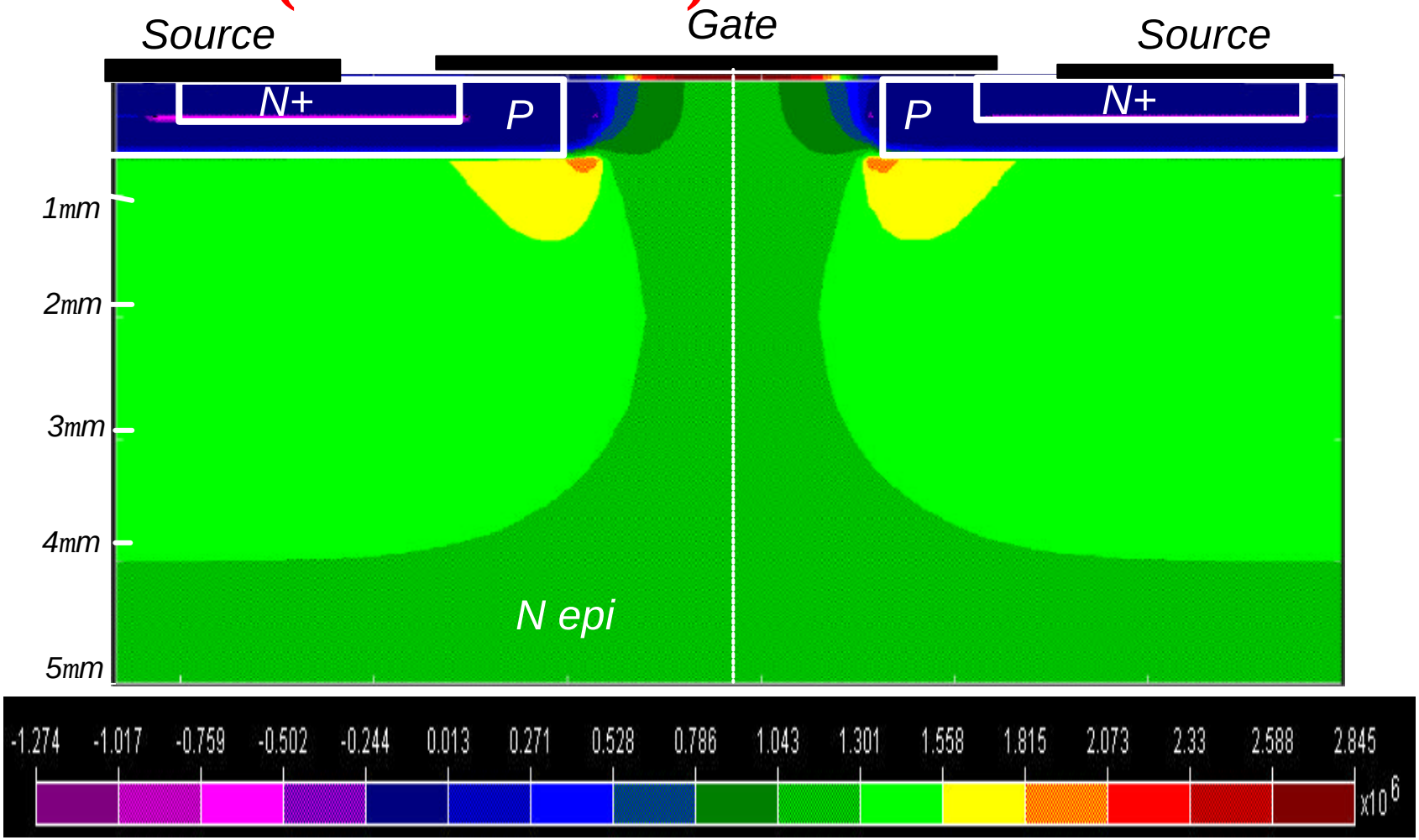
Nelson Saks

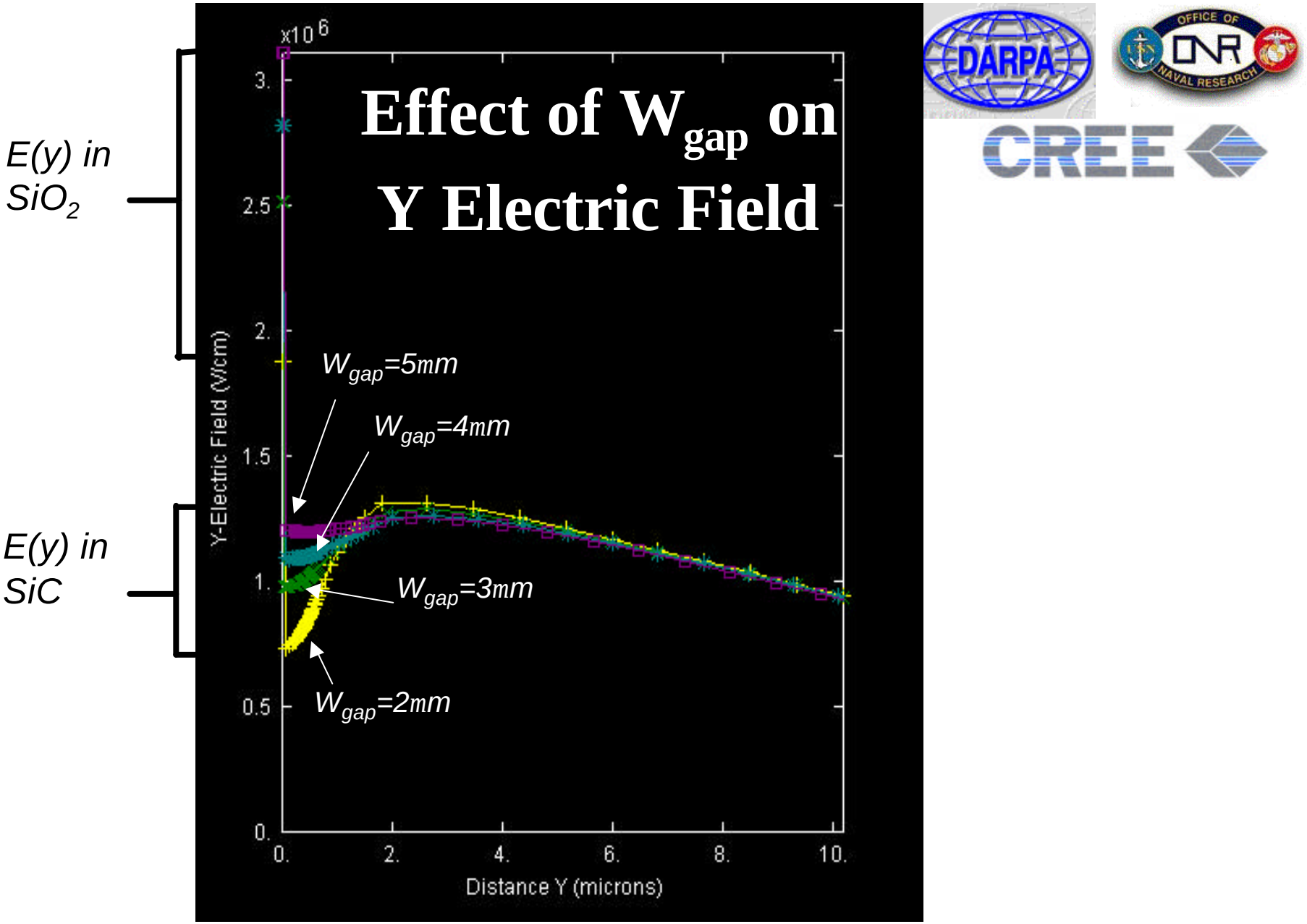
Implant Activation Sheet Resistivity

Dose=7.4×10^{12} cm^{-2}

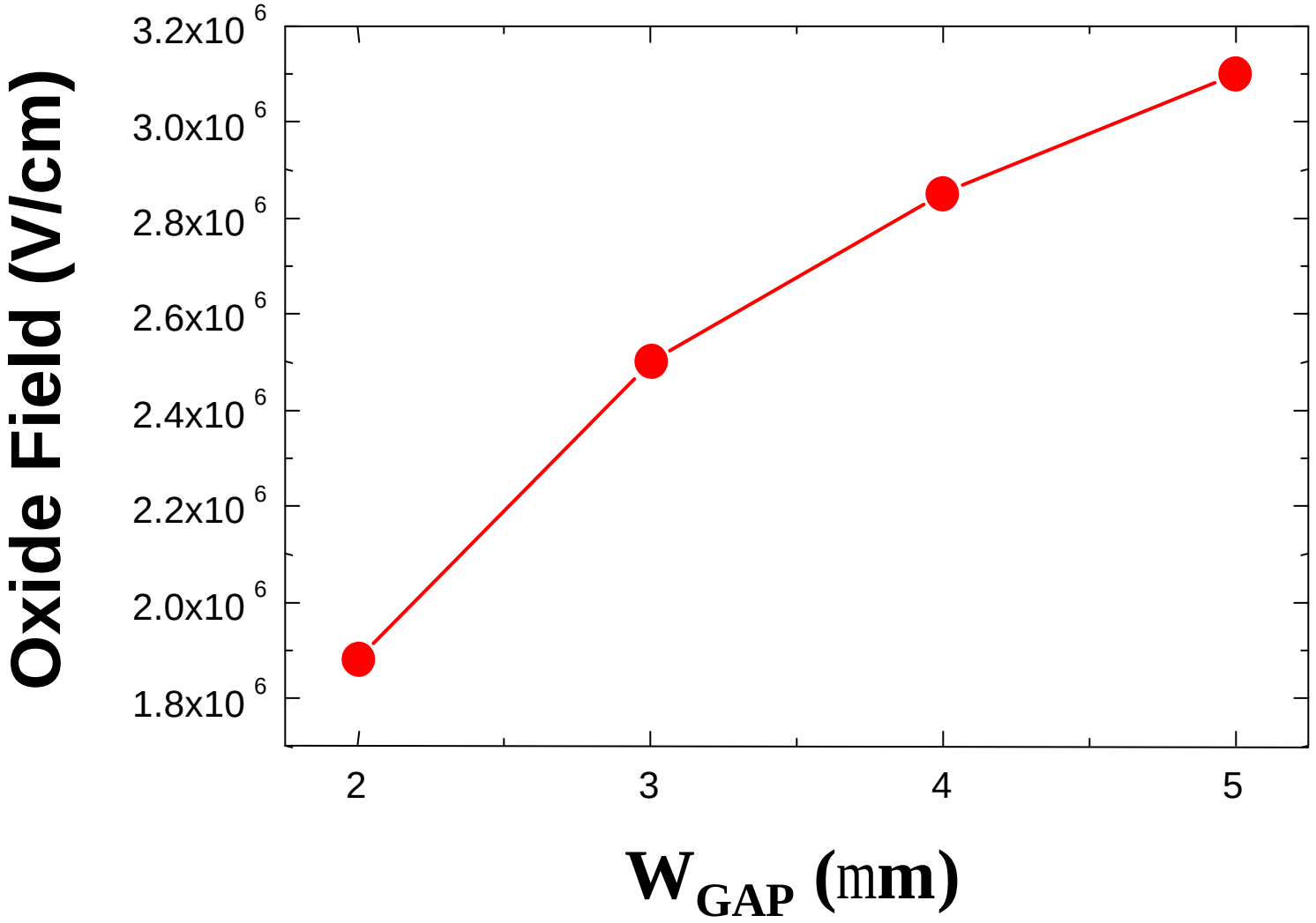


Off-State Simulation for W_{gap}=4mm device (Electric Field)

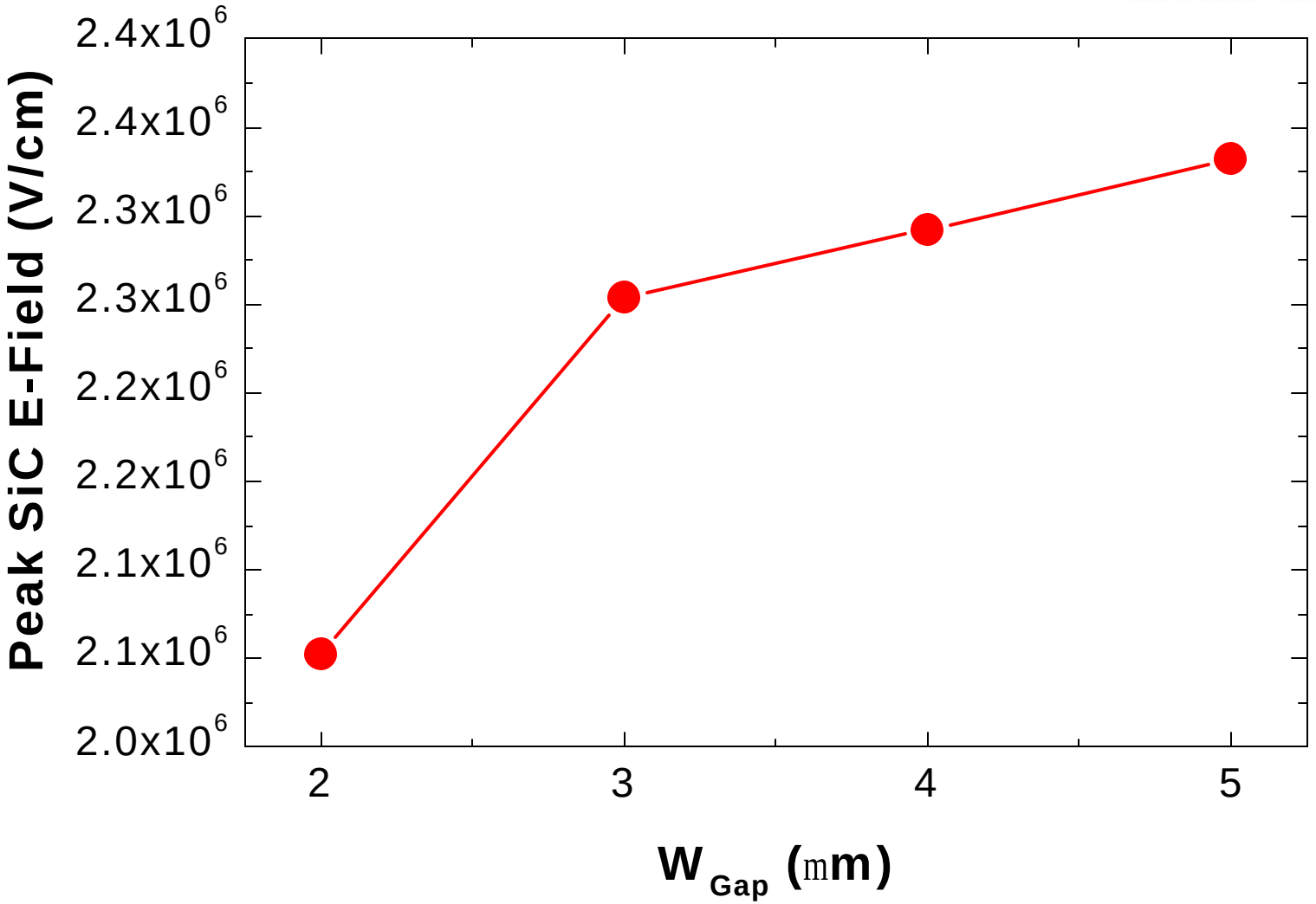



Effect of W_{gap} on Y Electric Field
E(y) in SiO_2
E(y) in SiC
x10 6
Y-Electric Field (V/cm)
Distance Y (microns)
W_{gap}=5mm
W_{gap}=4mm
W_{gap}=3mm
W_{gap}=2mm
0.
0.5
1.
1.5
2.
2.5
3.
0.
2.
4.
6.
8.
10.

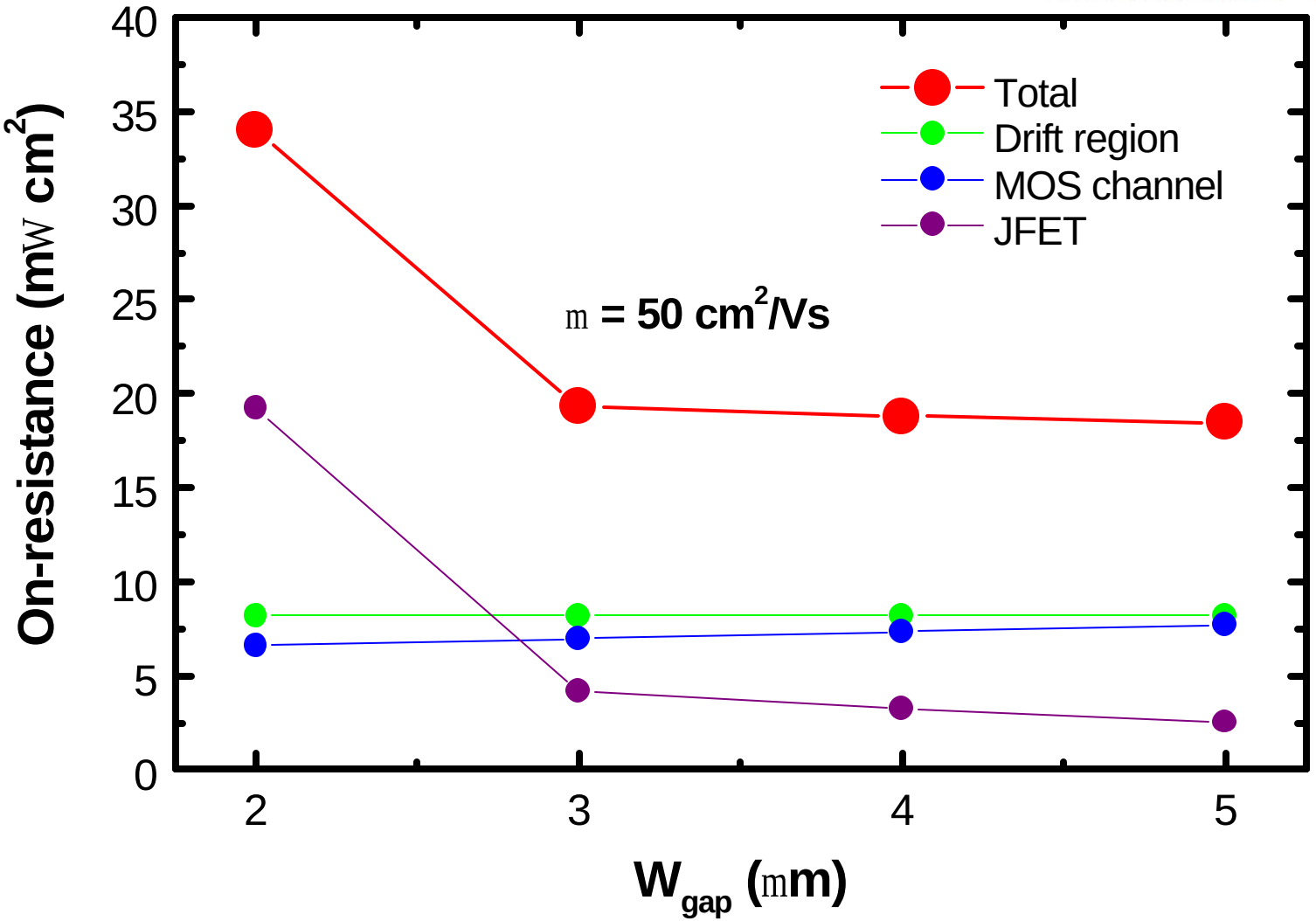
Effect of W_{gap} on Oxide Electric Field (4H)



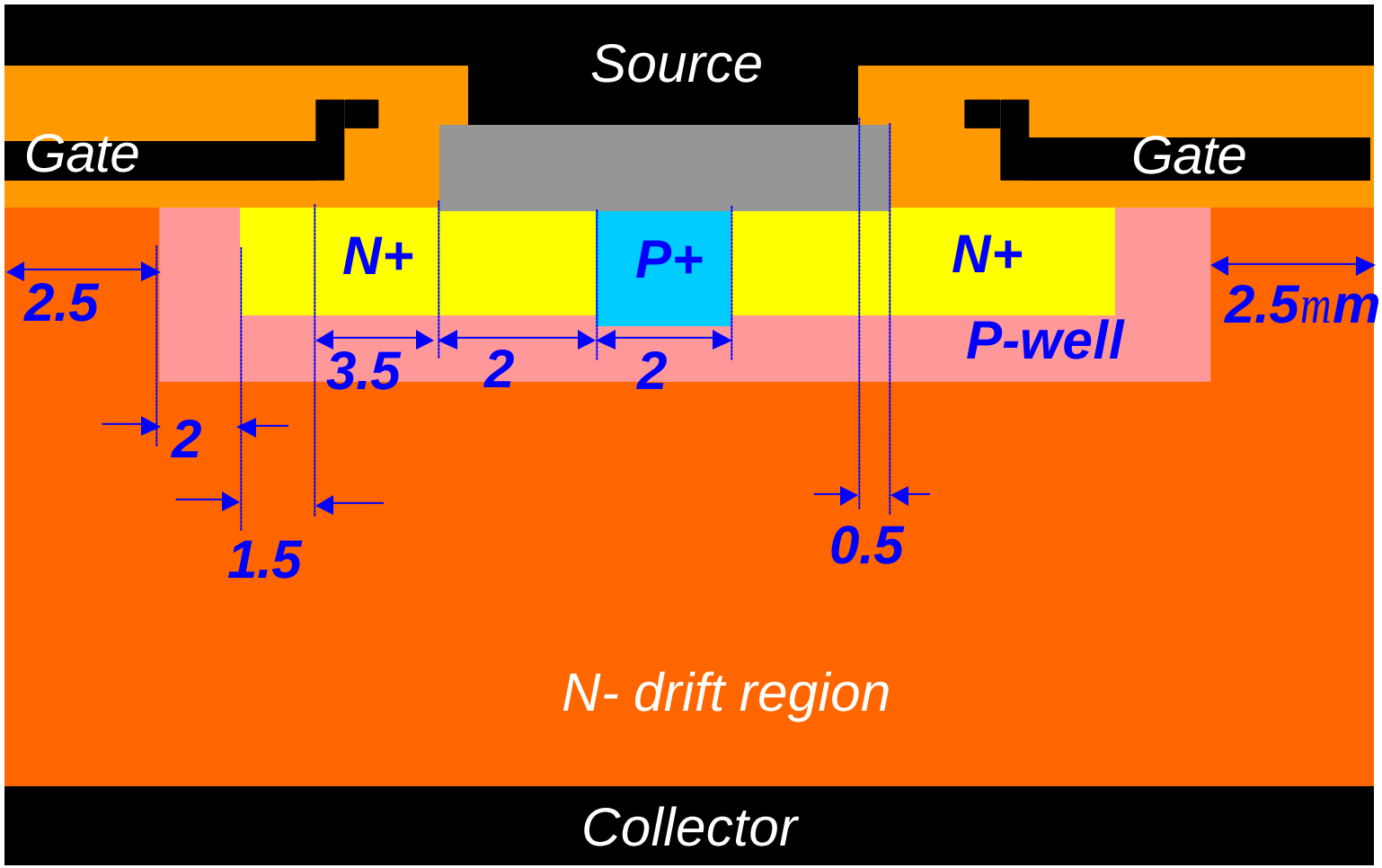
Peak E field in Silicon Carbide (4H)



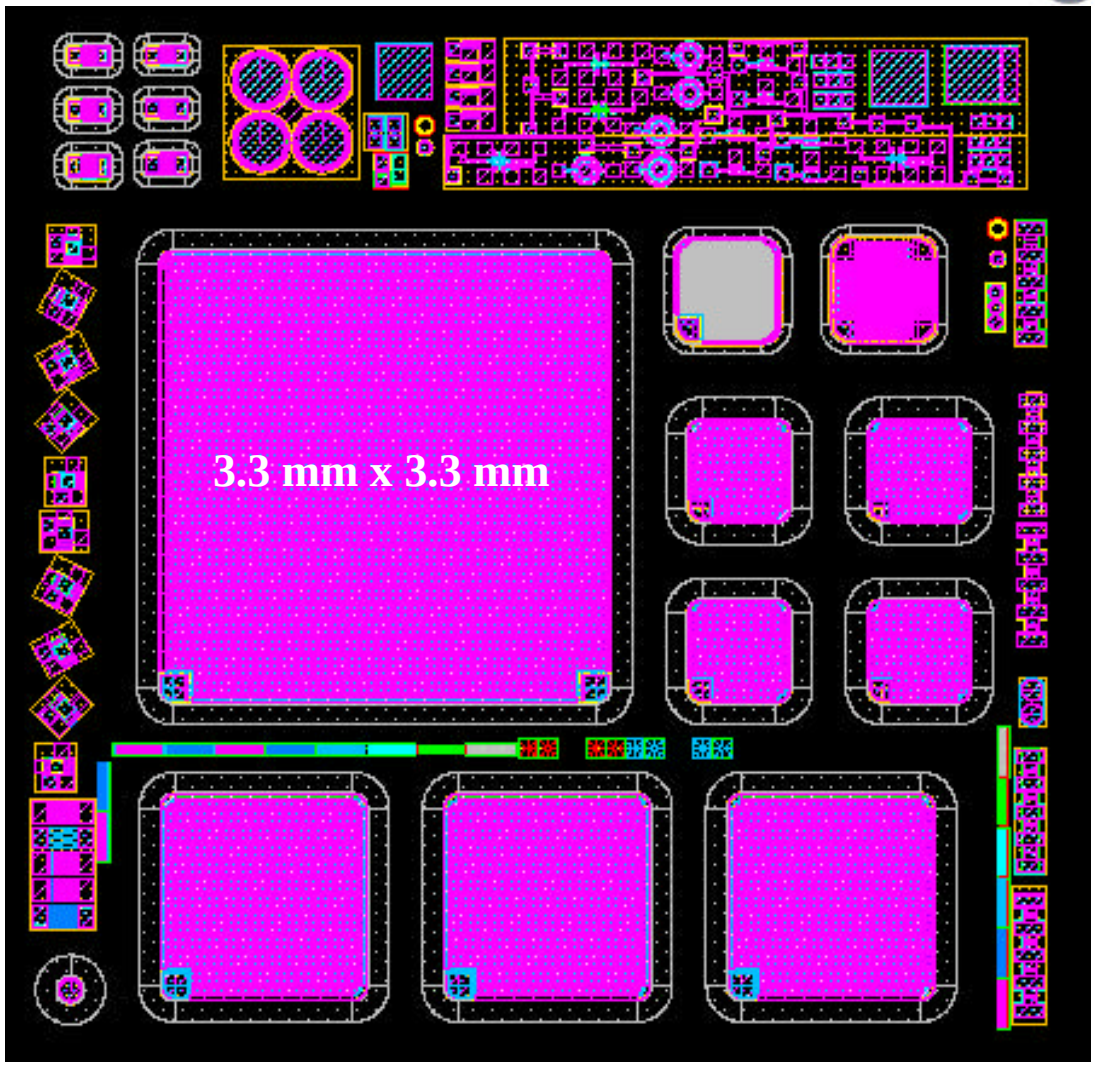
Effect of W_{gap} on On-resistance (4H)



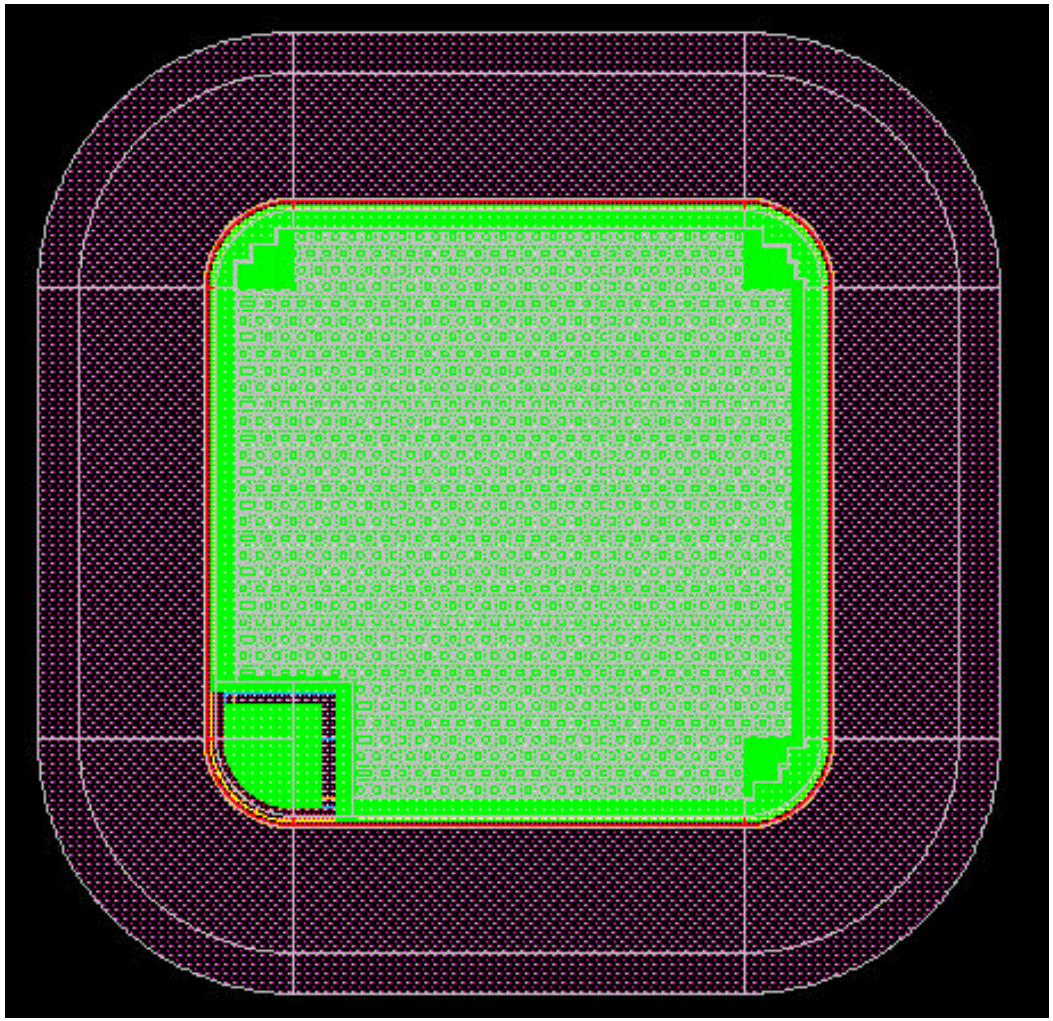
Standard Cell cross-section



Chip Layout
7.5mm x 7.5mm)



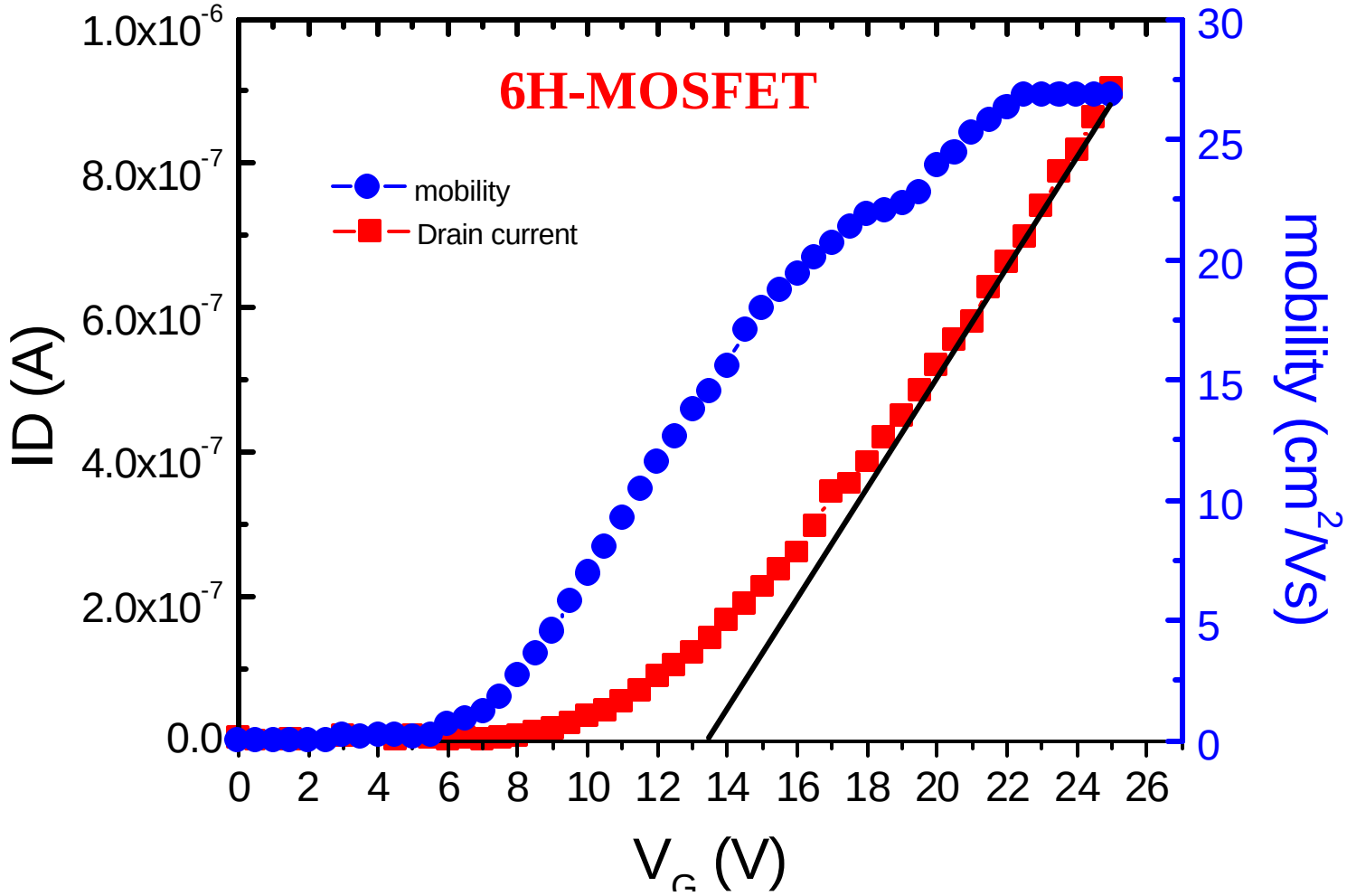
0.75 mm x 0.75 mm MOSFET



Before BC implant

(W/L=100㎜/100㎜)

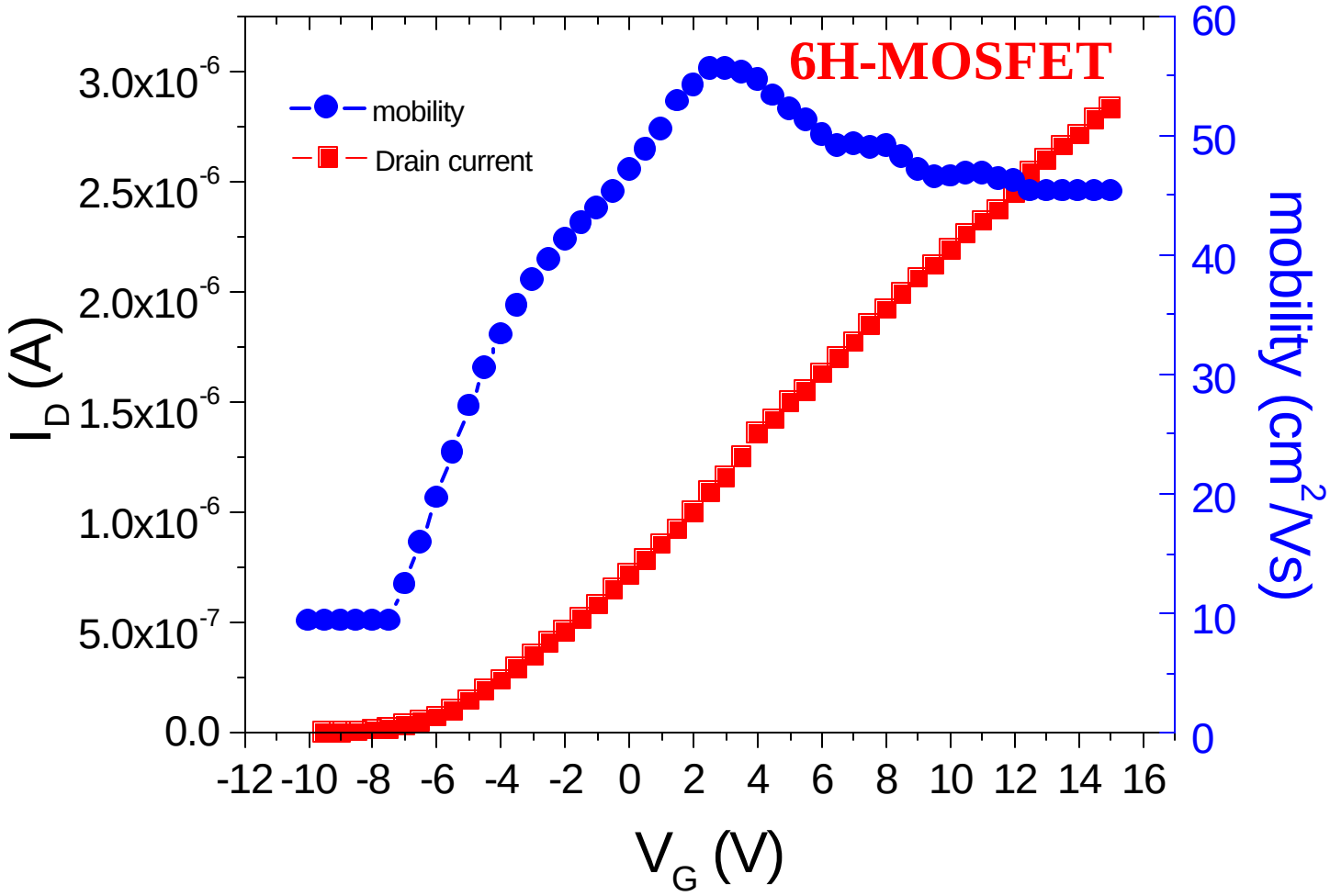
Deposited Oxide, 1100°C dry-1 hr, 950°C Dry ReOx-3 hrs



After BC implant

($4.0x10^{12}$ cm^{-2}, W/L=100㎜/100㎜)

Deposited Oxide, 1100°C dry-1 hr, 950°C Dry ReOx-3 hrs

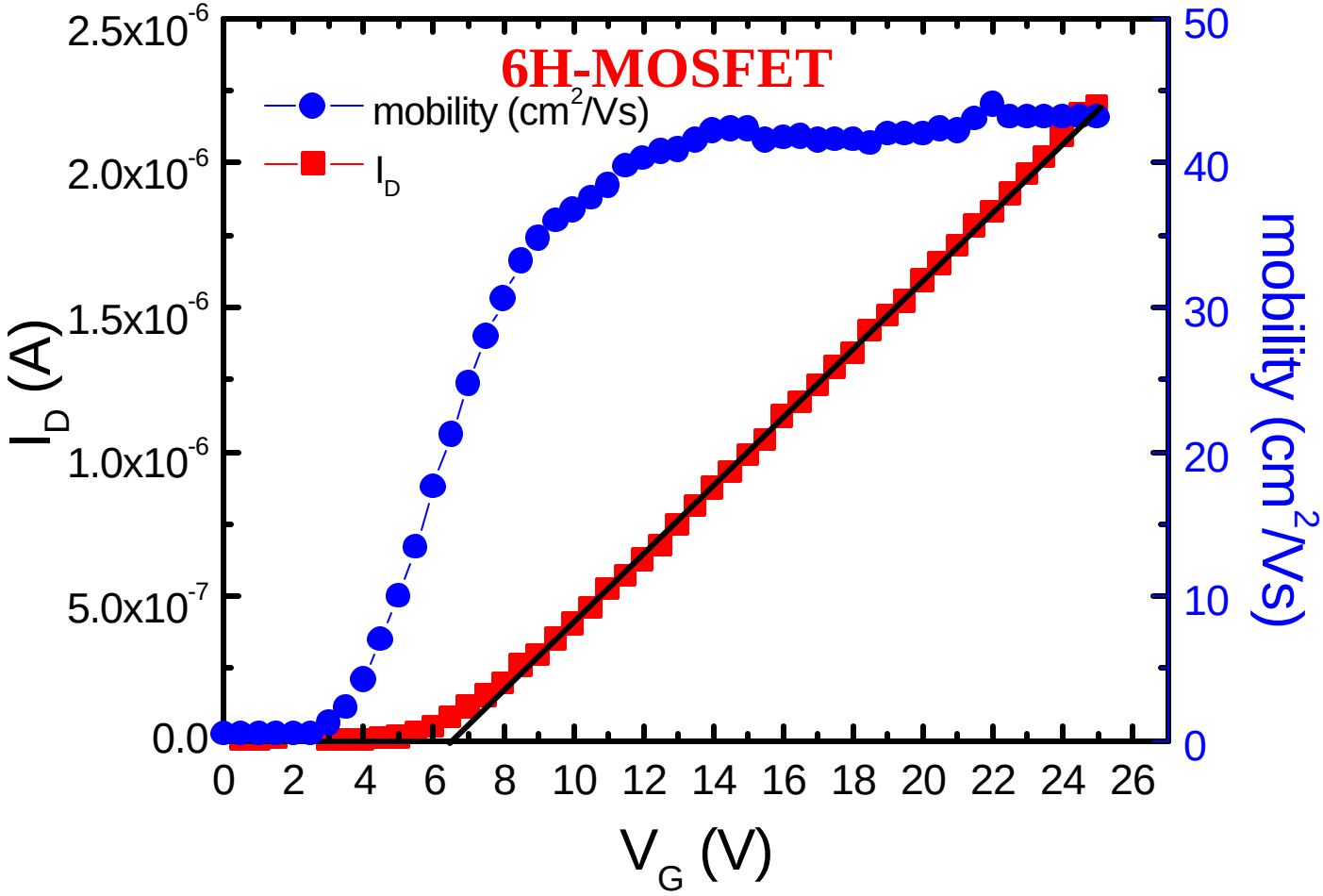


After BC implant

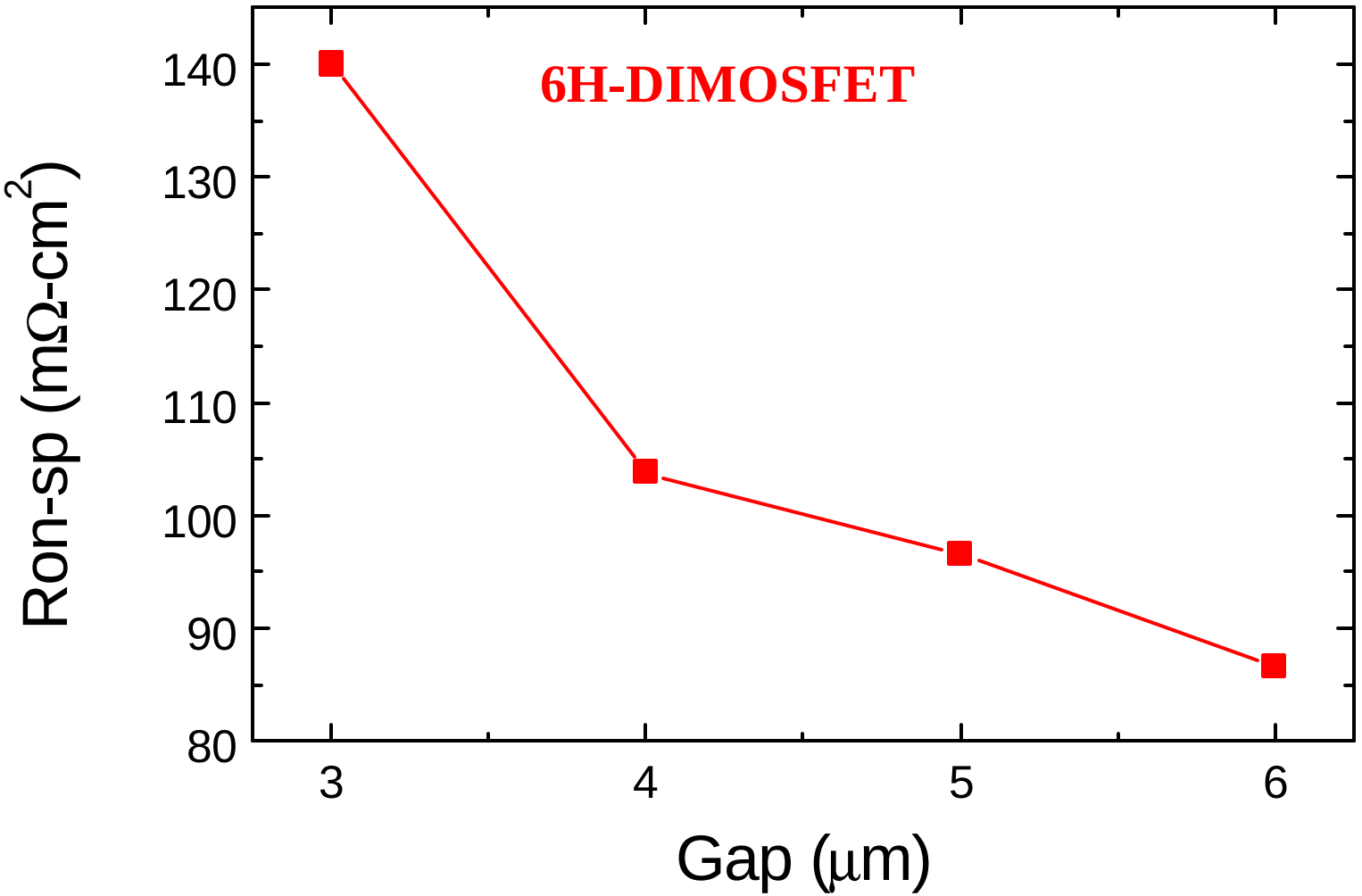
($2.0x10^{12}$ cm^{-2}, W/L=100㎜/100㎜)

CREE

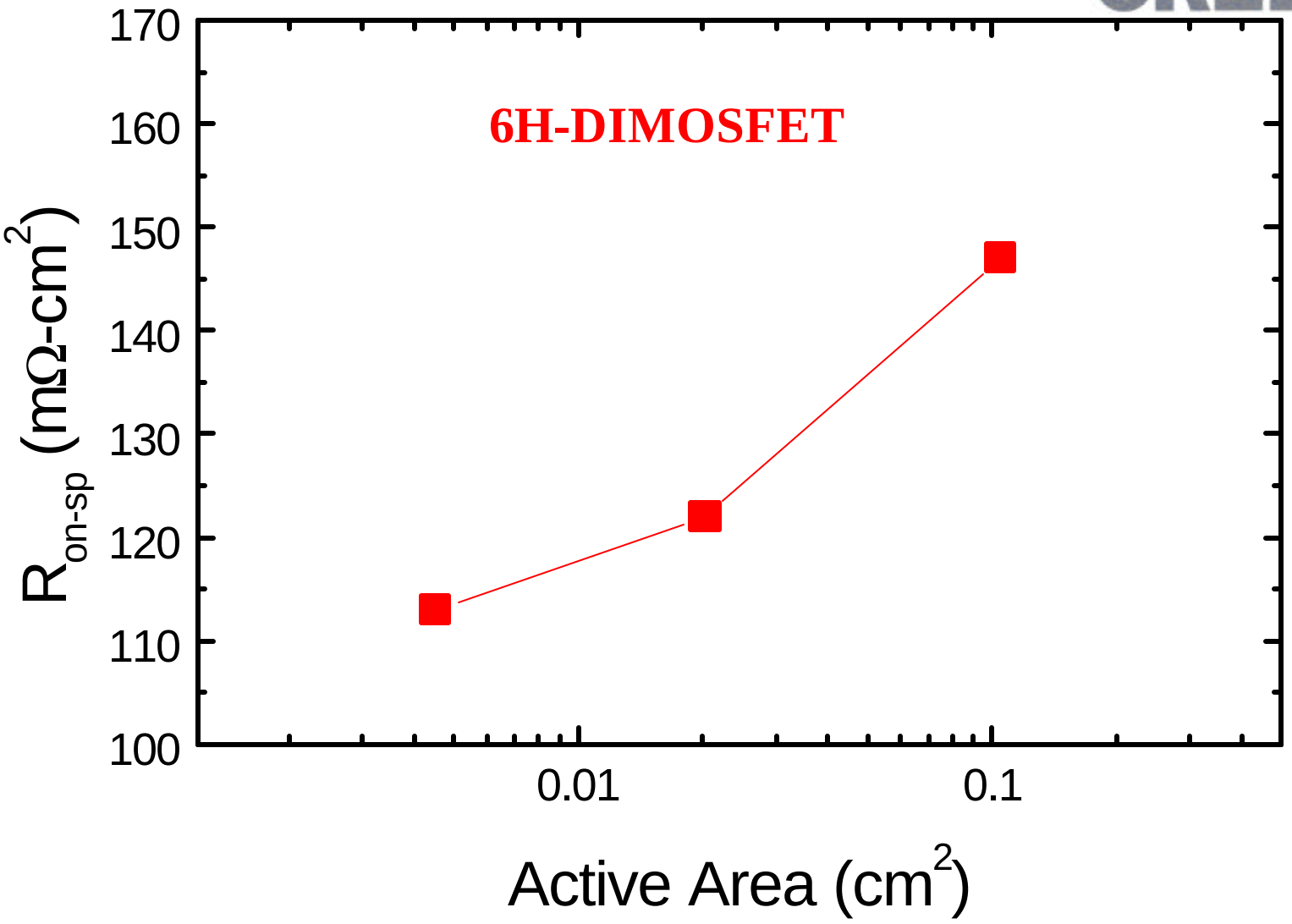
Deposited Oxide, 1100°C dry-1 hr, 950°C Dry ReOx-3 hrs



Effect of JFET gap on specific on-resistance



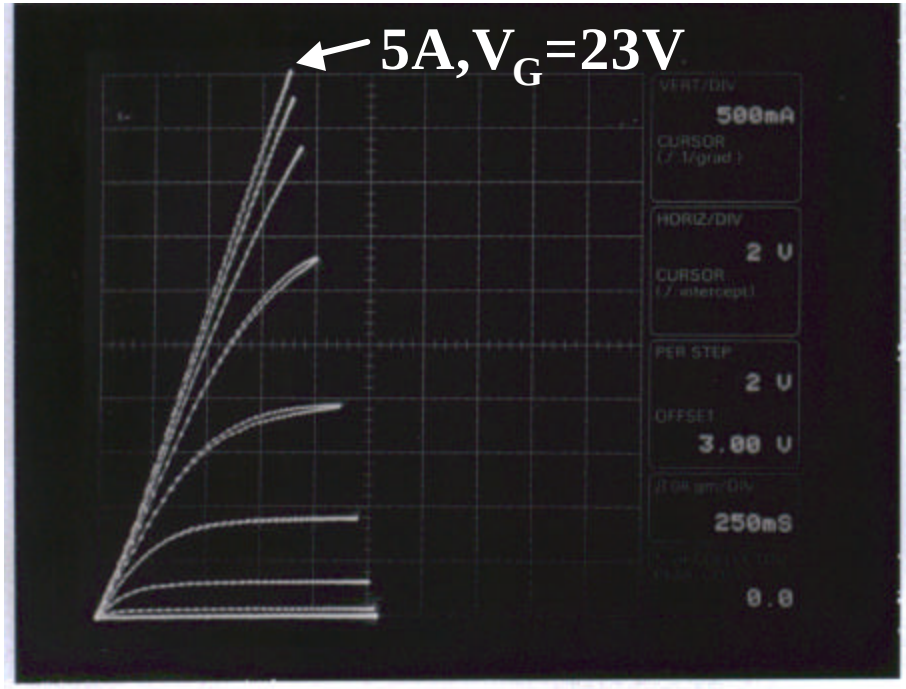
Effect of device active area on specific on-resistance



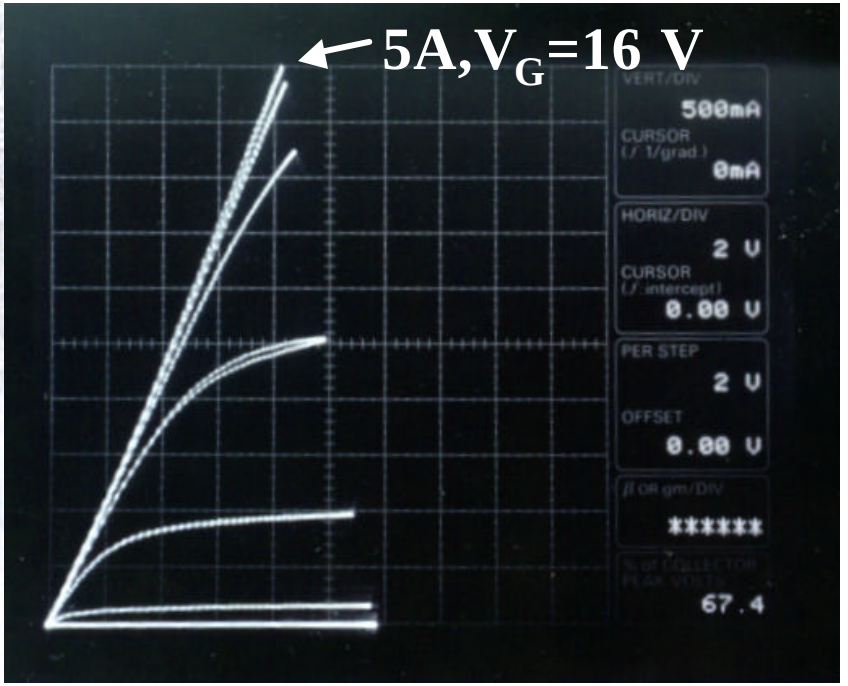
3.3 mm x 3.3 mm 6H-SiC DIMOSFET

(active area=0.105 cm^2, JFETgap=5 mm)

Deposited Oxide, 1100°C dry-1 hr, 950°C Dry ReOx-3 hrs



No BC implant



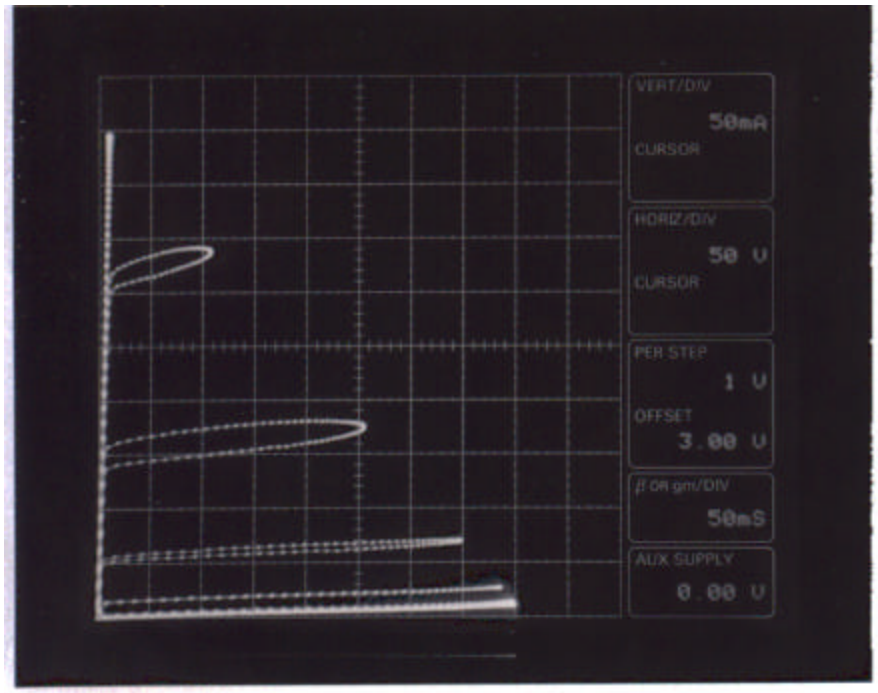
With BC implant

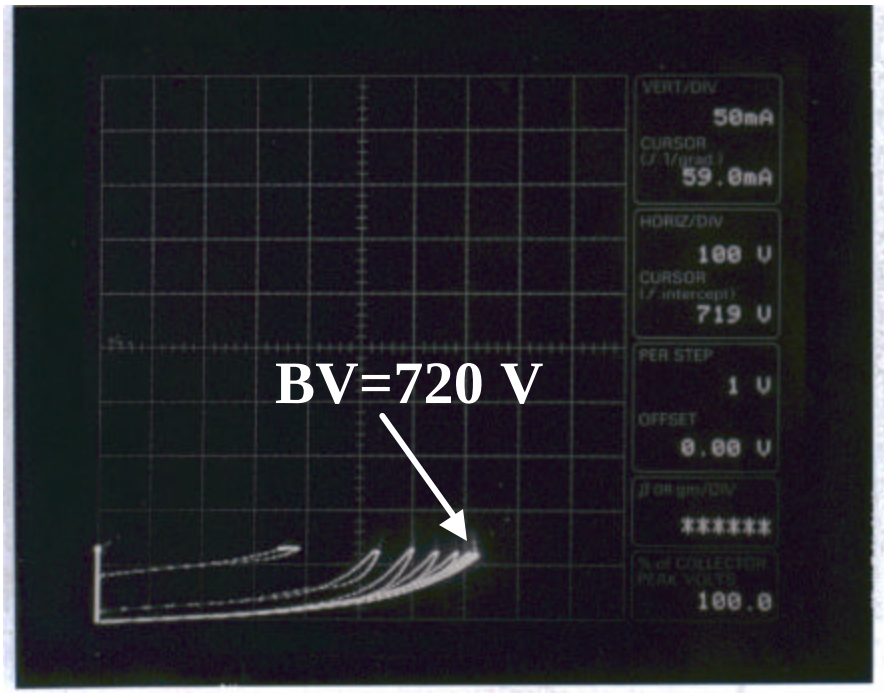
2.0x10^{12} cm^{-2}

3.3 mm x 3.3 mm 6H-SiC MOSFET Blocking characteristics

(no BC implant, active area=0.105 cm^2, JFET gap=4.5 mm)

Deposited Oxide, 1100°C dry-1 hr, 950°C Dry ReOx-3 hrs

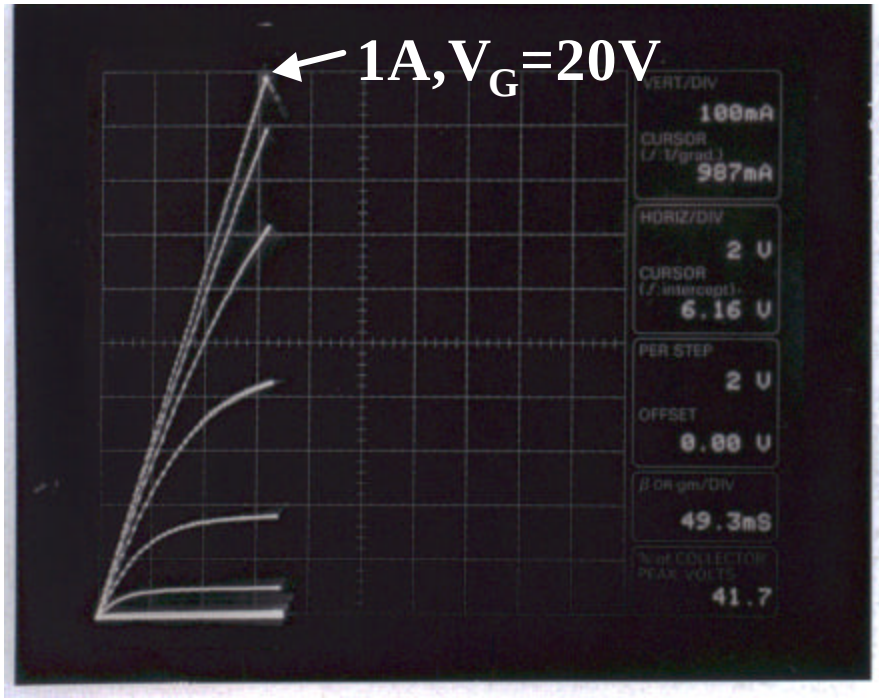


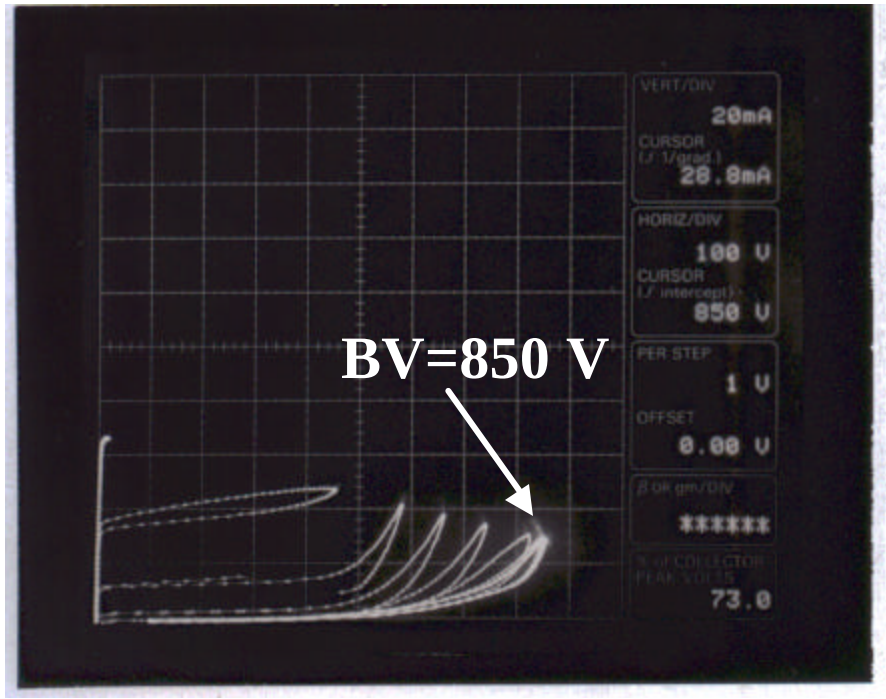


1.5 mm x 1.5 mm 6H-SiC MOSFET

(no BC implant, active area=0.02027 cm^2, JFET gap=4.5 mm)

Deposited Oxide, 1100°C dry-1 hr, 950°C Dry ReOx-3 hrs

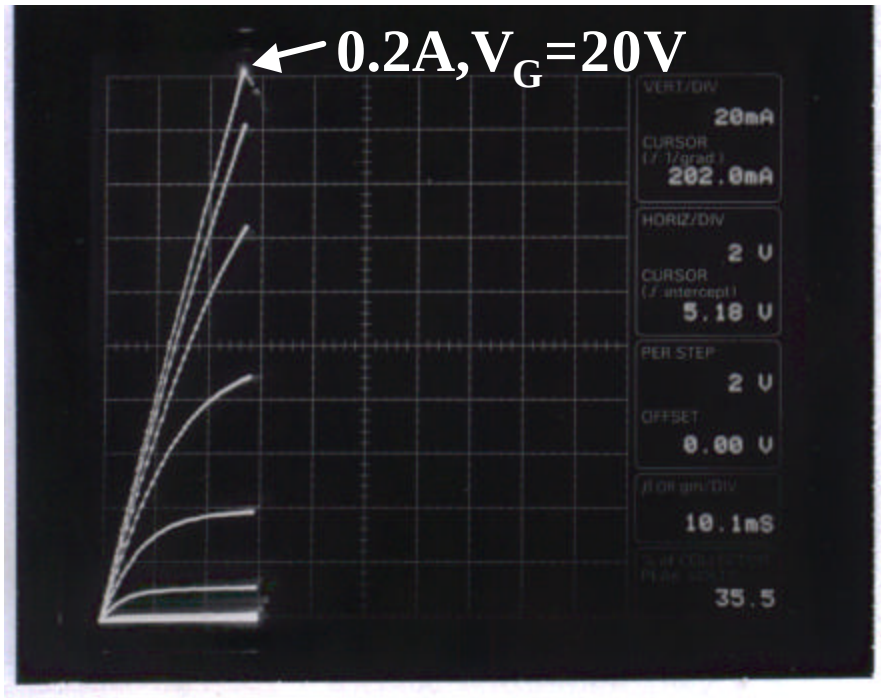


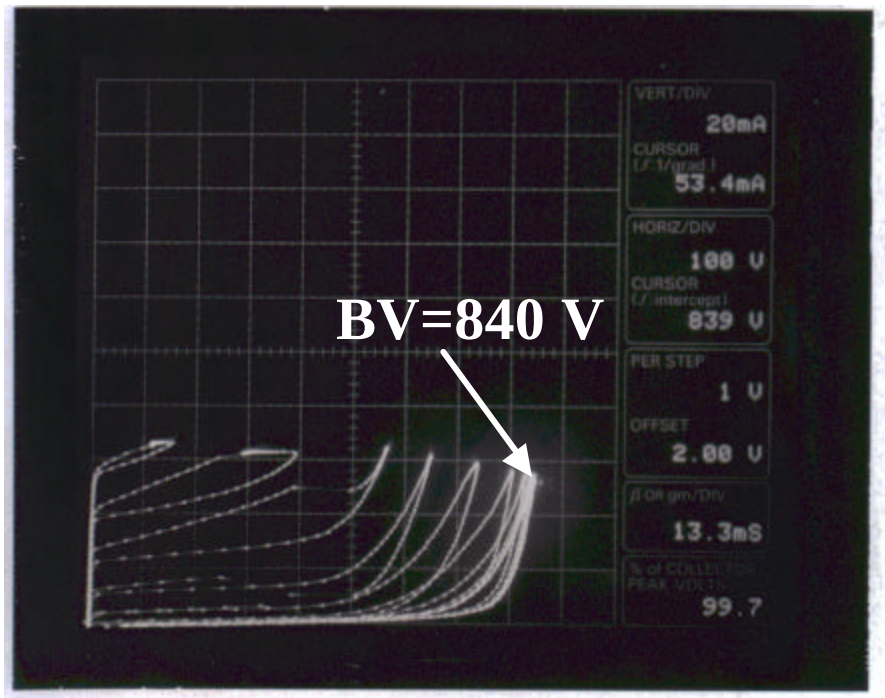


0.75 mm x 0.75 mm 6H-SiC DIMOSFET

(no BC implant, active area=0.00453 cm^2, JFET gap=4.5 μm)

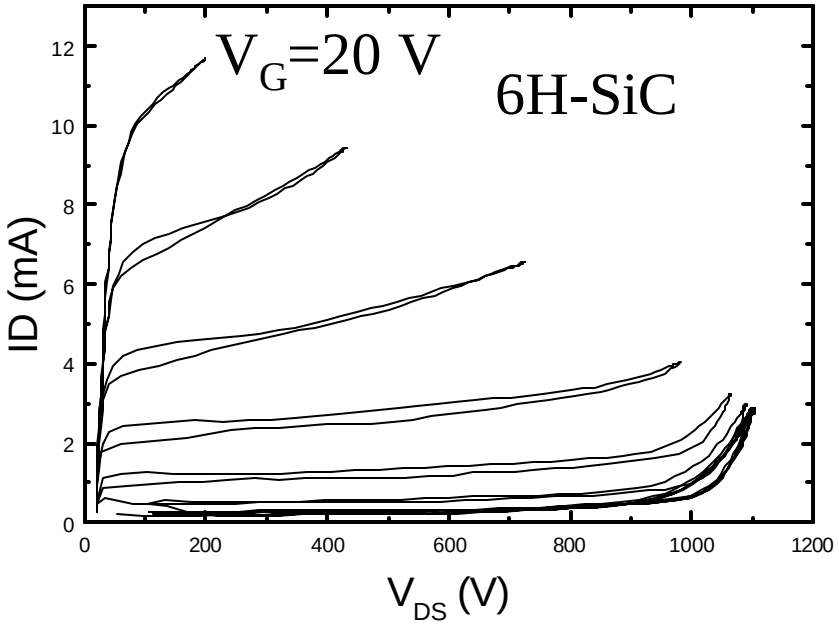
Deposited Oxide, 1100°C dry-1 hr, 950°C Dry ReOx-3 hrs



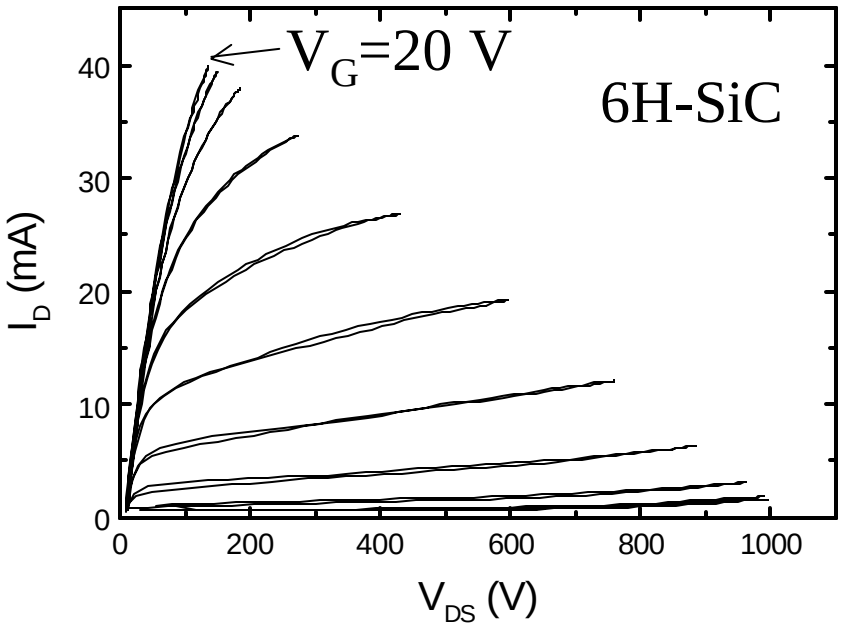


Breakdown Characteristics of small DIMOSFET test cells (3㎜ JFET gap)

Deposited Oxide, 1100°C dry-1 hr, 950°C Dry ReOx-3 hrs



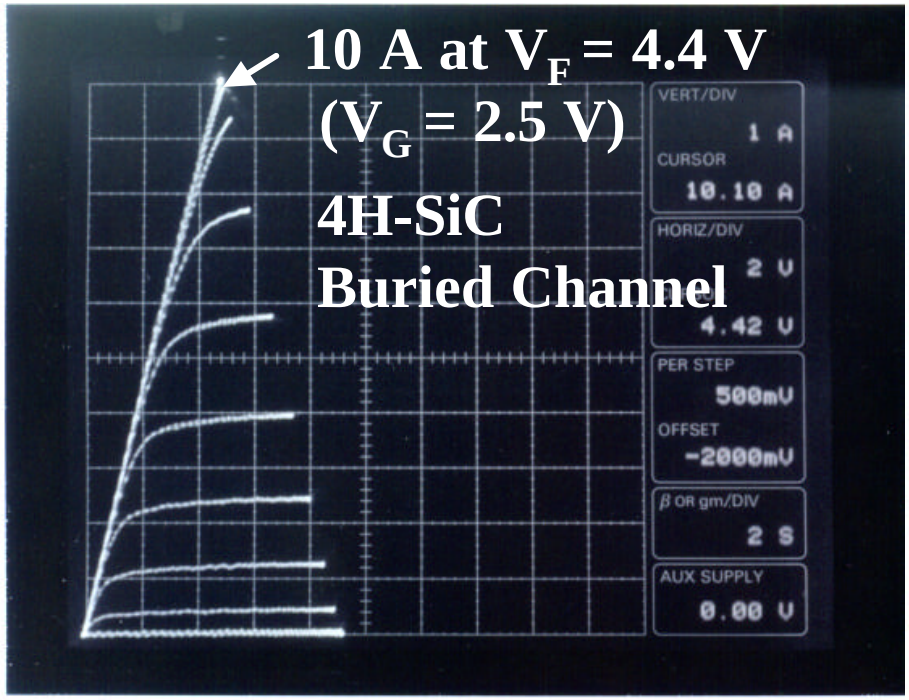
No BC implant

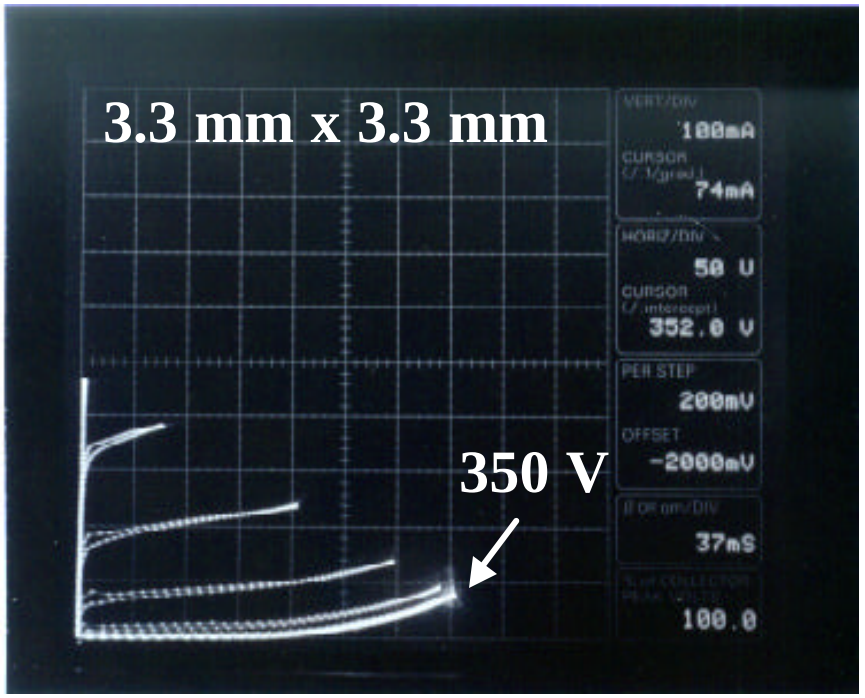


With BC implant

$2.0x10^{12}$ cm^{-2}

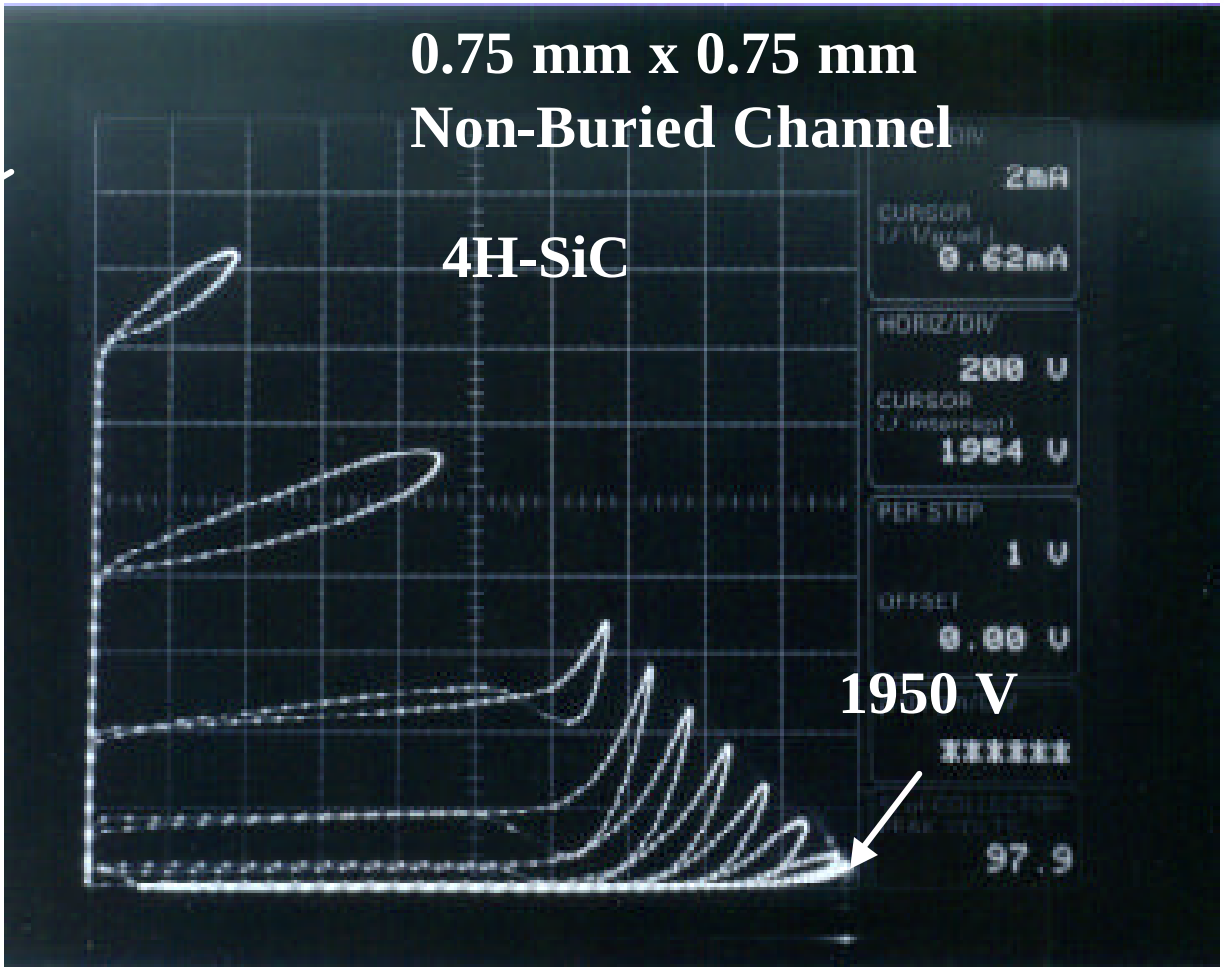
3.3 mm x 3.3 mm 4H-SiC Power MOSFET produces 10 A



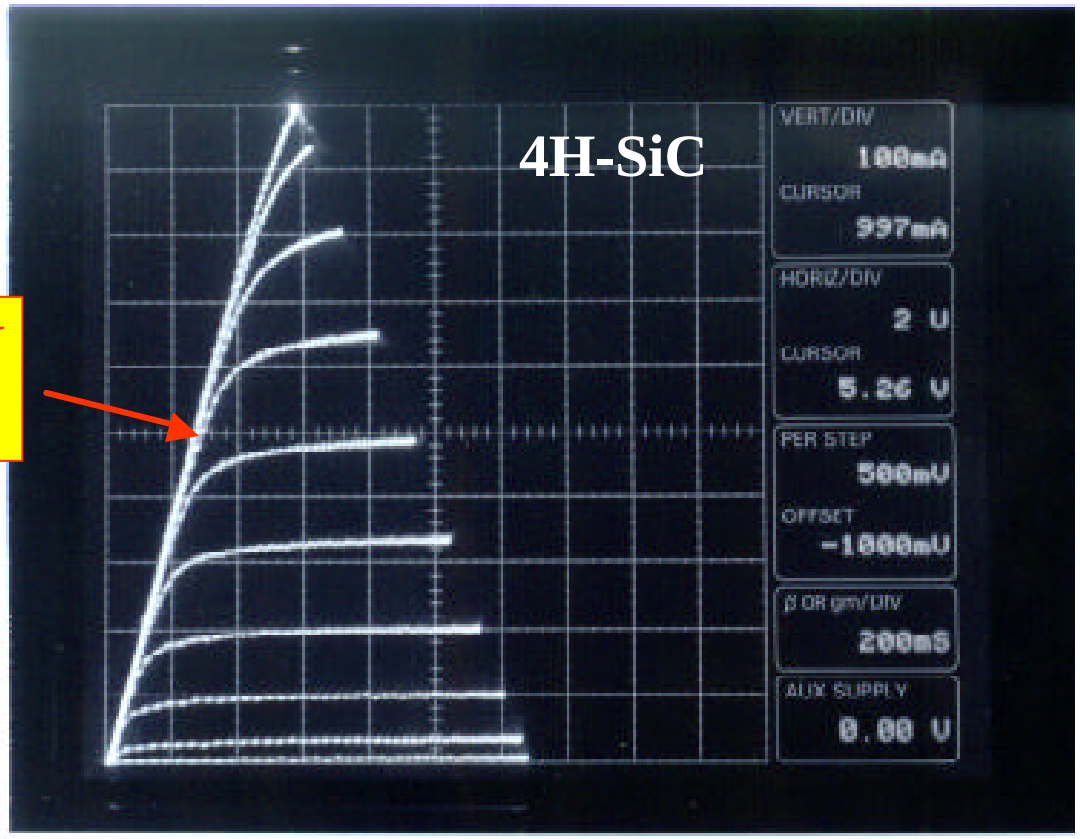


R_{ON} = 43 mohm.cm^2 (Pitch = 25 mm)

0.75 mm x 0.75 mm 4H-SiC Power MOSFET can block 1950 V



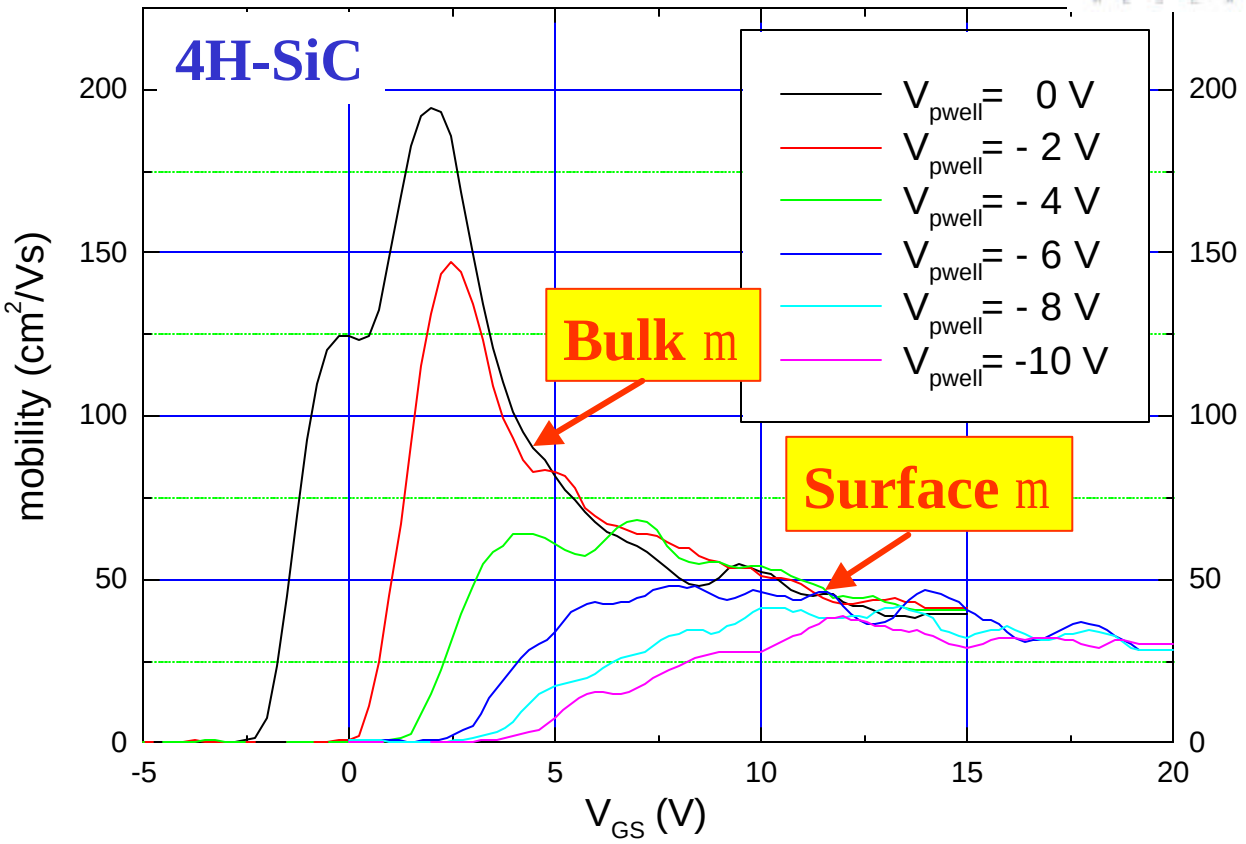
0.75 mm x 0.75 mm chip with a smaller pitch (16 mm) reduces the on-resistance



0.5 A at V_F = 2.6 V (V_G = 4 V)

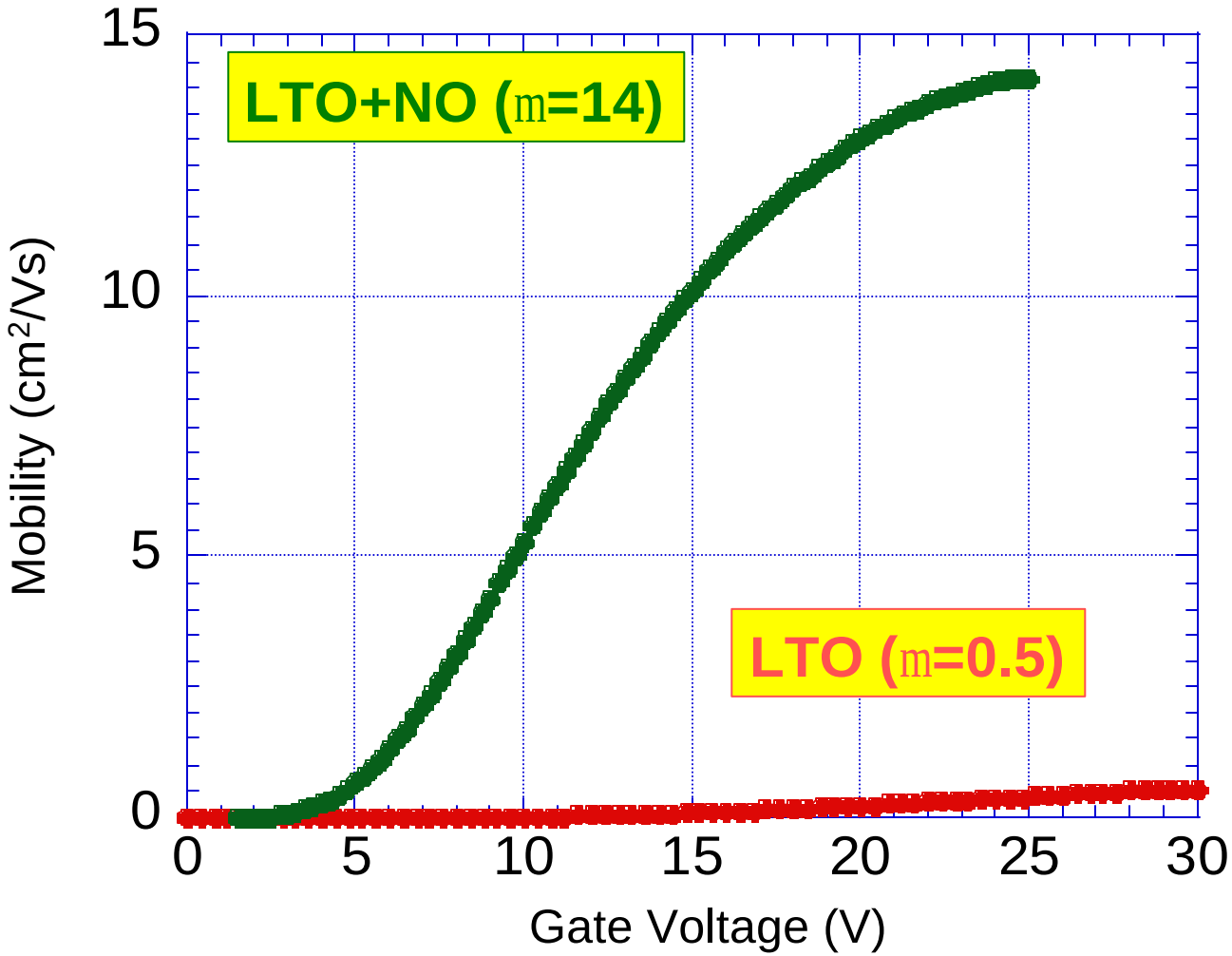
R_{ON} = 23 mohm.cm^2 (Pitch = 16 mm)

Extracted effective electron mobility as a function of reverse p-well bias



The buried channel charge can be adjusted for normally-off operation

Effect of NO Anneal on Deposited Oxide



Conclusions

- **Buried Channel devices show good promise.**
- **NO anneal for 4H-SiC needs further optimization.**

Summary

- **2A @ V_f=3V, 720V, 6H-SiC DiMOSFET (Non-Buried Channel) demonstrated**
- **10A@ V_f = 4.4V, 350V, 4H-SiC DiMOSFET demonstrated (Buried Channel)**
- **Peak Mobility of 195 cm^2/Vs for 4H-SiC Buried Channel demonstrated**