Silicon Carbide Power Electronics: An enabler for future DoD systems

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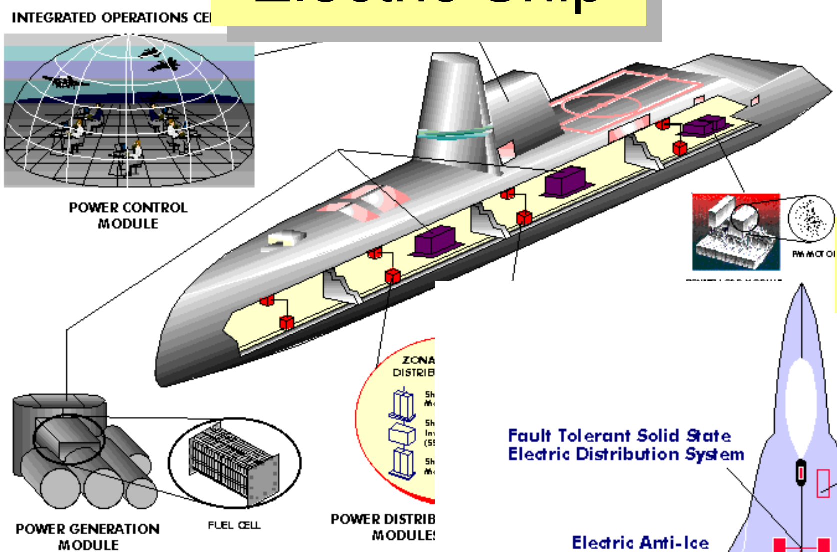
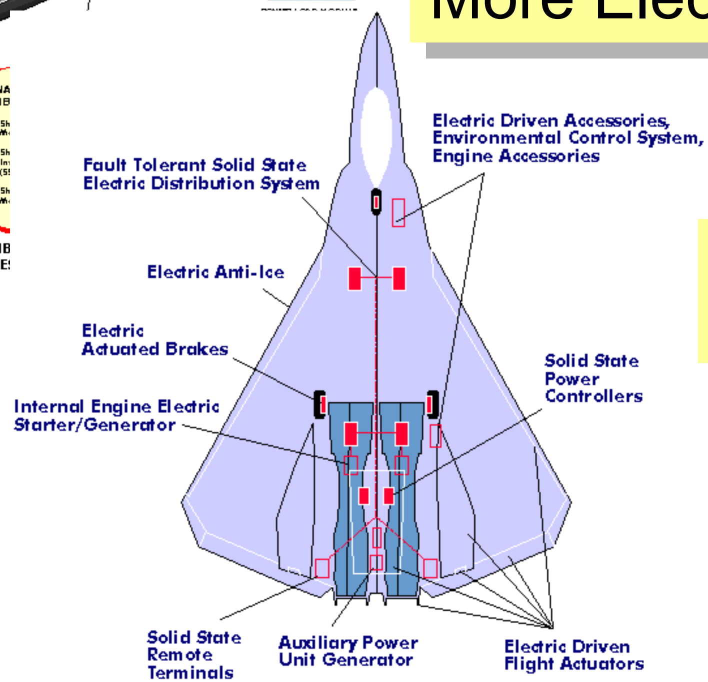
RPI SiC Symposium

Services are moving towards electric platforms .....

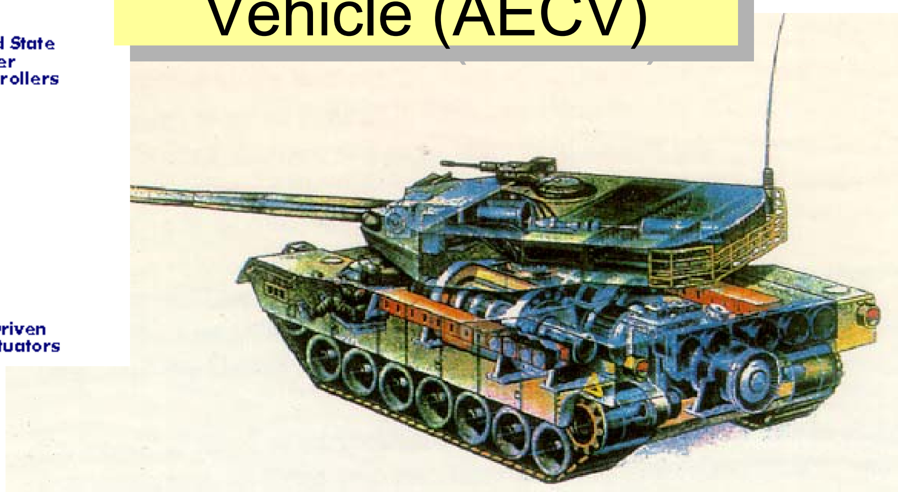
Electric Ship



More Electric Aircraft



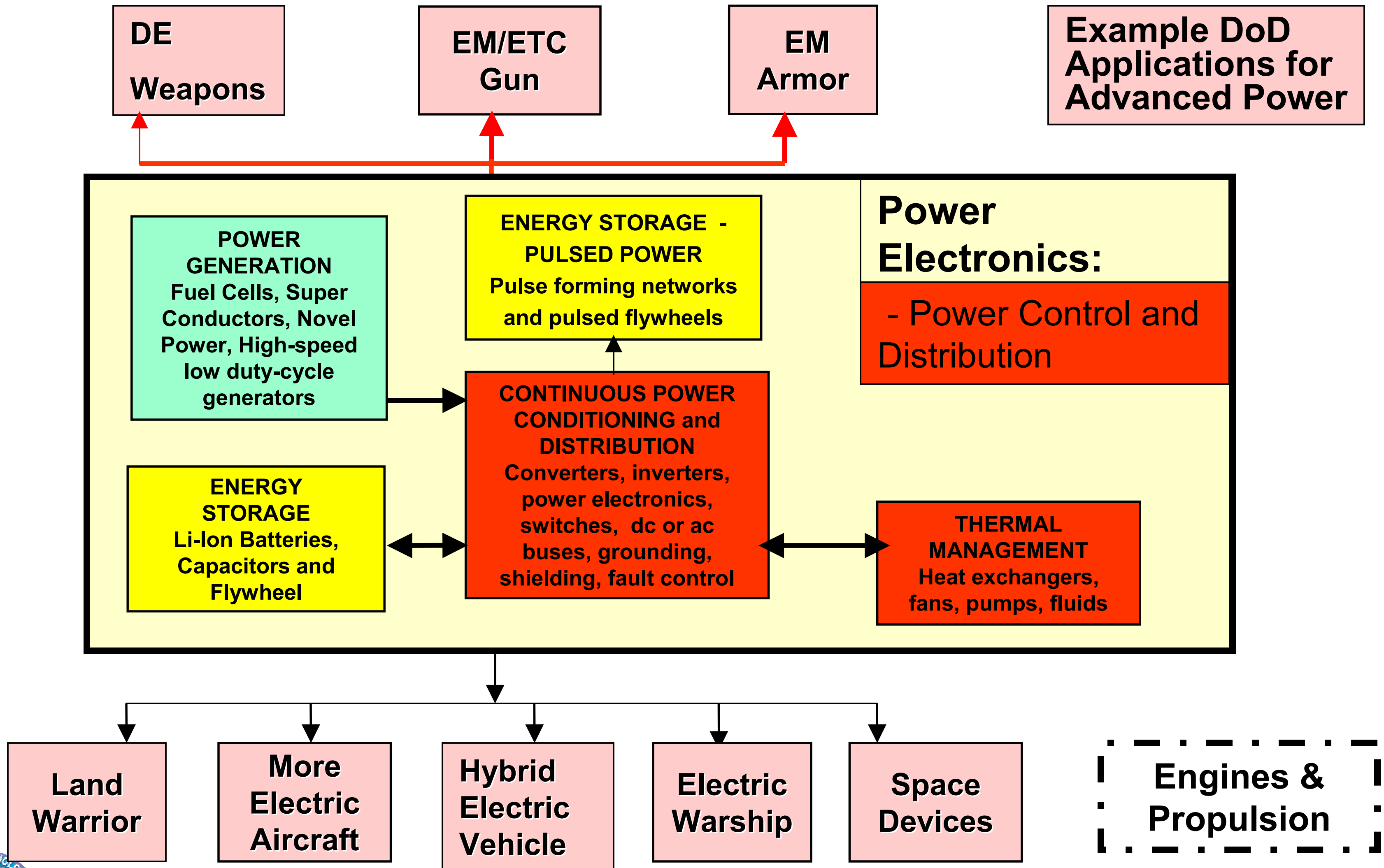
All Electric Combat Vehicle (AECV)



…. but current solid state power conversion technology limits system performance in:

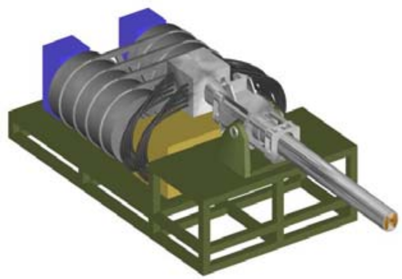
- Size
- Weight
- Complexity
- Efficiency
- Noise

Component Technologies Enable System Capabilities

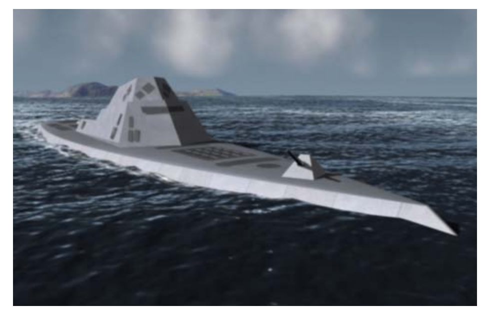


Multiple Platforms for EM Gun

- Army:
  - Armored Fighting Vehicles
  - Air Defense
  - Artillery



- Marines:
  - MEFFV

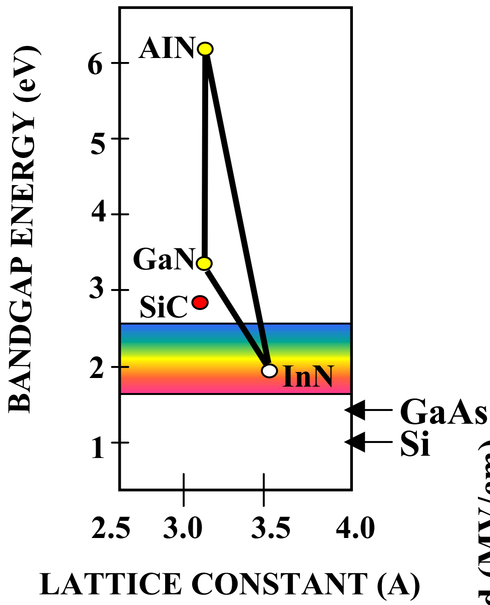


- Navy: DDX
  - Ship Defense
  - Long Range Fire Support

- Air Force: AC130
  - Standoff
  - Precision

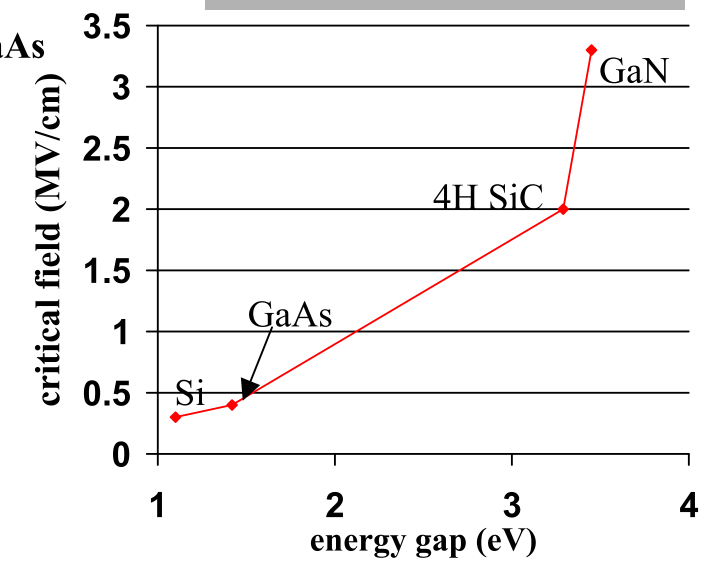
Enabling Properties of WBS

bandgap for optical emission



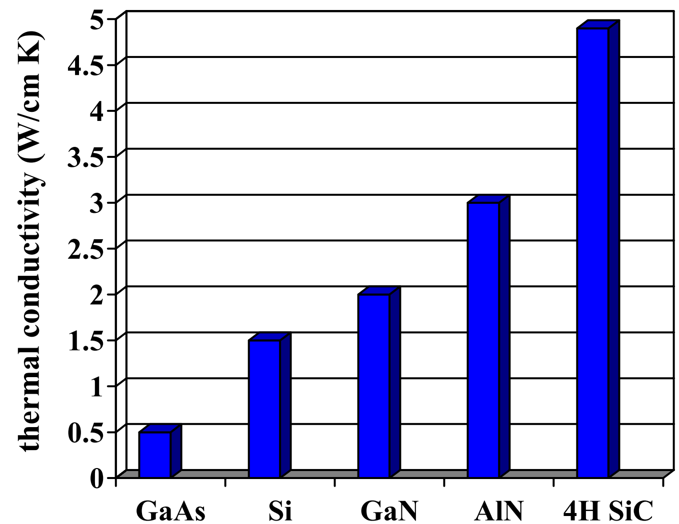
Short wavelength light emitting diodes, lasers, and detectors

critical electric field 10x Si and GaAs



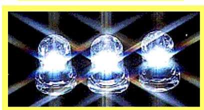
High voltage operation

SiC thermal conductivity 7x GaAs



High power operation

Wide Bandgap Semiconductors: Opening New Solid State Applications



- opto-electronic market continues to grow (>$1.4B in FY02)
  - blue, green, UV LEDs and lasers (signage, sensors, optical storage)
  - Solid State White Lighting: DoE pushing for solid state lighting initiative (potential >$20B/yr market, US industry opportunity to re-enter lighting market)

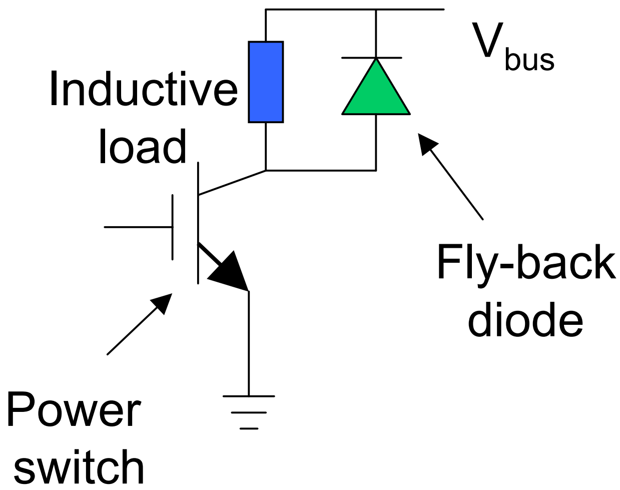
- Initial power and microwave devices entering market:
  - 600 V SiC Schottky rectifiers in market from two suppliers
  - 2 GHz SiC MESFET driver chip being sampled

- Increased interest in Asia and Europe for GaN RF electronics and SiC power electronics.

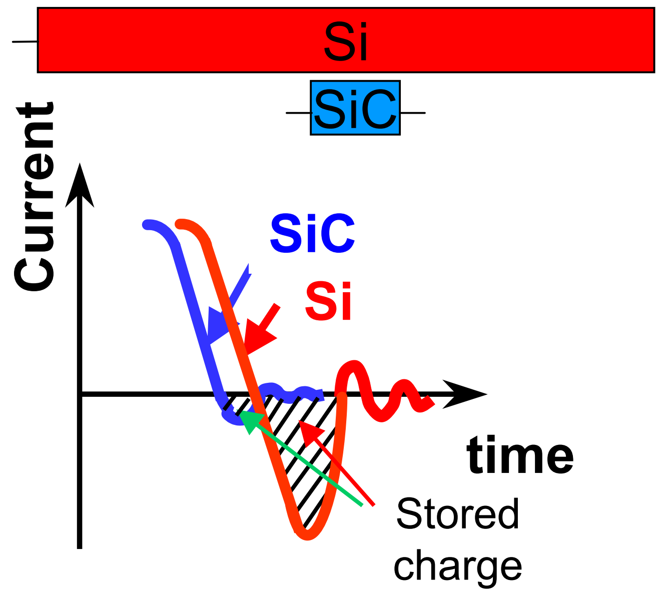
- US continues to lead world in WBG electronics material and devices.

SiC Switching Advantage

- Lower on-resistance
- Lower switching loss
- Higher switching frequency



Motor Drive



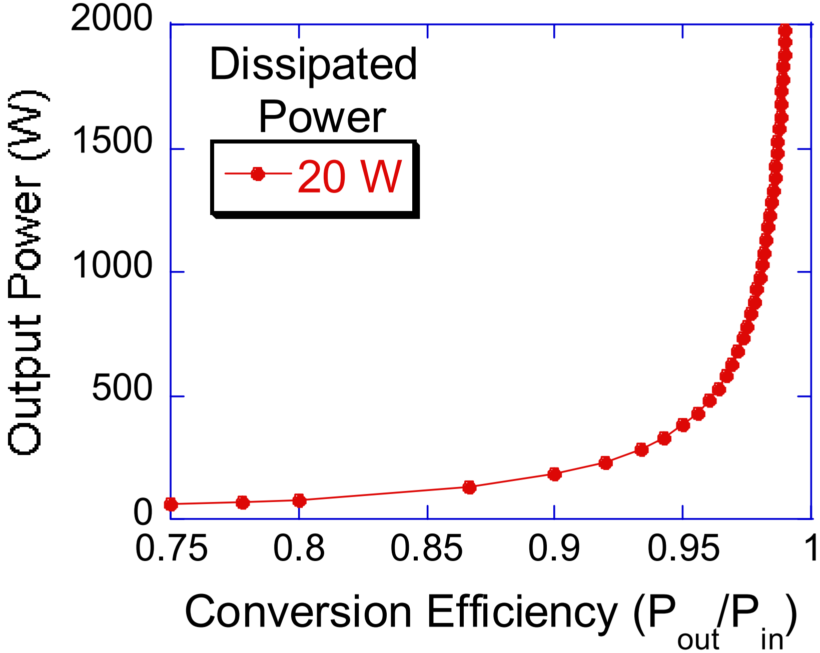
Diode switching characteristics

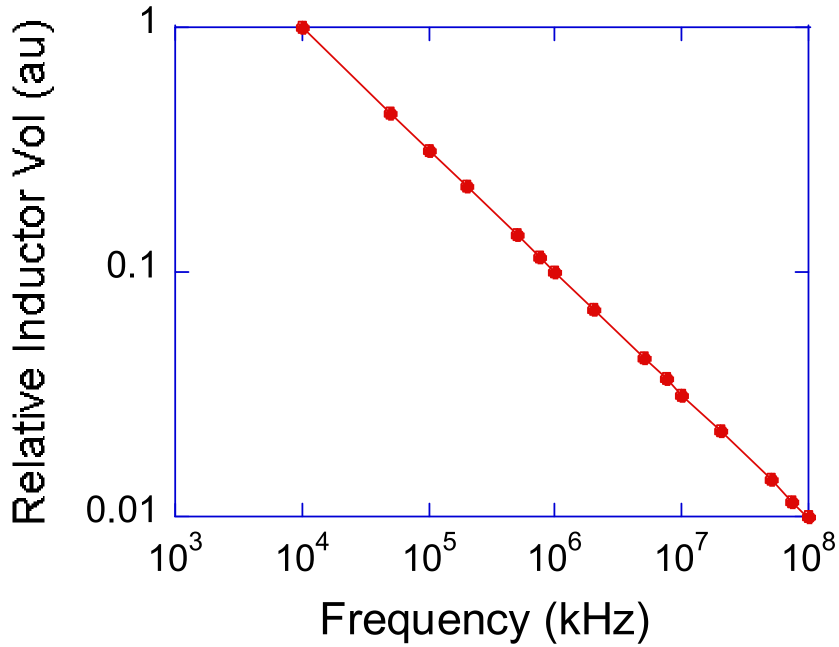
<u>SiC for 600 V inductive load</u>:
7x reduced peak reverse current
5x reduced recovery time
4x reduced switching energy

Impact of Increased Efficiency and Frequency

$$P_{out} = \frac{efficiency \times P_{dis}}{1 - efficiency}$$

$$InductorVol \propto \frac{1}{\sqrt{freq}}$$





Assumption: fixed power dissipation

Increase available power with smaller volume

Wide Bandgap Semiconductor Technology Initiative

Thrust Area I: RF/Microwave/Millimeter-wave Technology

Radar

Space-based Sensors and communication systems

Decoys, jammers, seekers

Thrust Area II: High Power Electronic Technology

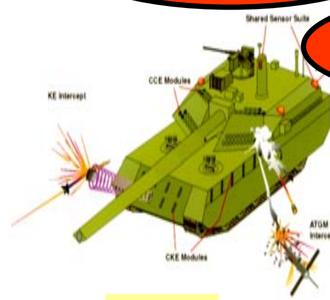
More Electric Aircraft/UAV

High Voltage 1 - 25kV

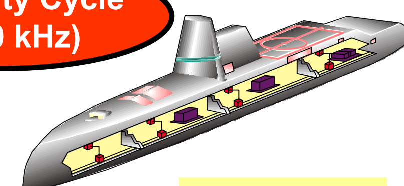
High Current ~ 1kA/cm^2

High Temperature (>300 °C)

High Duty Cycle (>100 kHz)



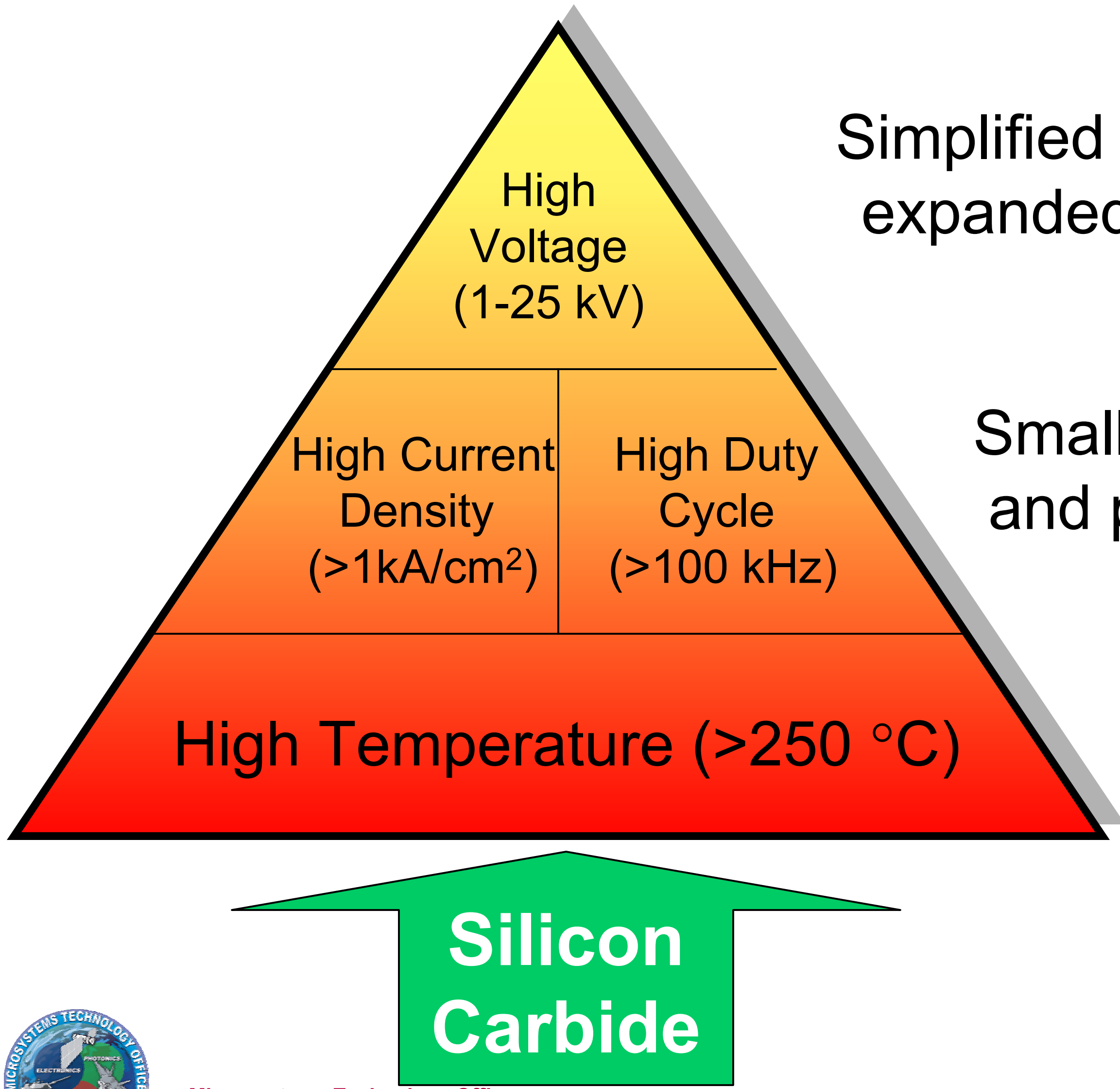
FCS



Electric Ship

John Zolper
Edgar Martinez

Wide Bandgap High Power Electronics (HPE)

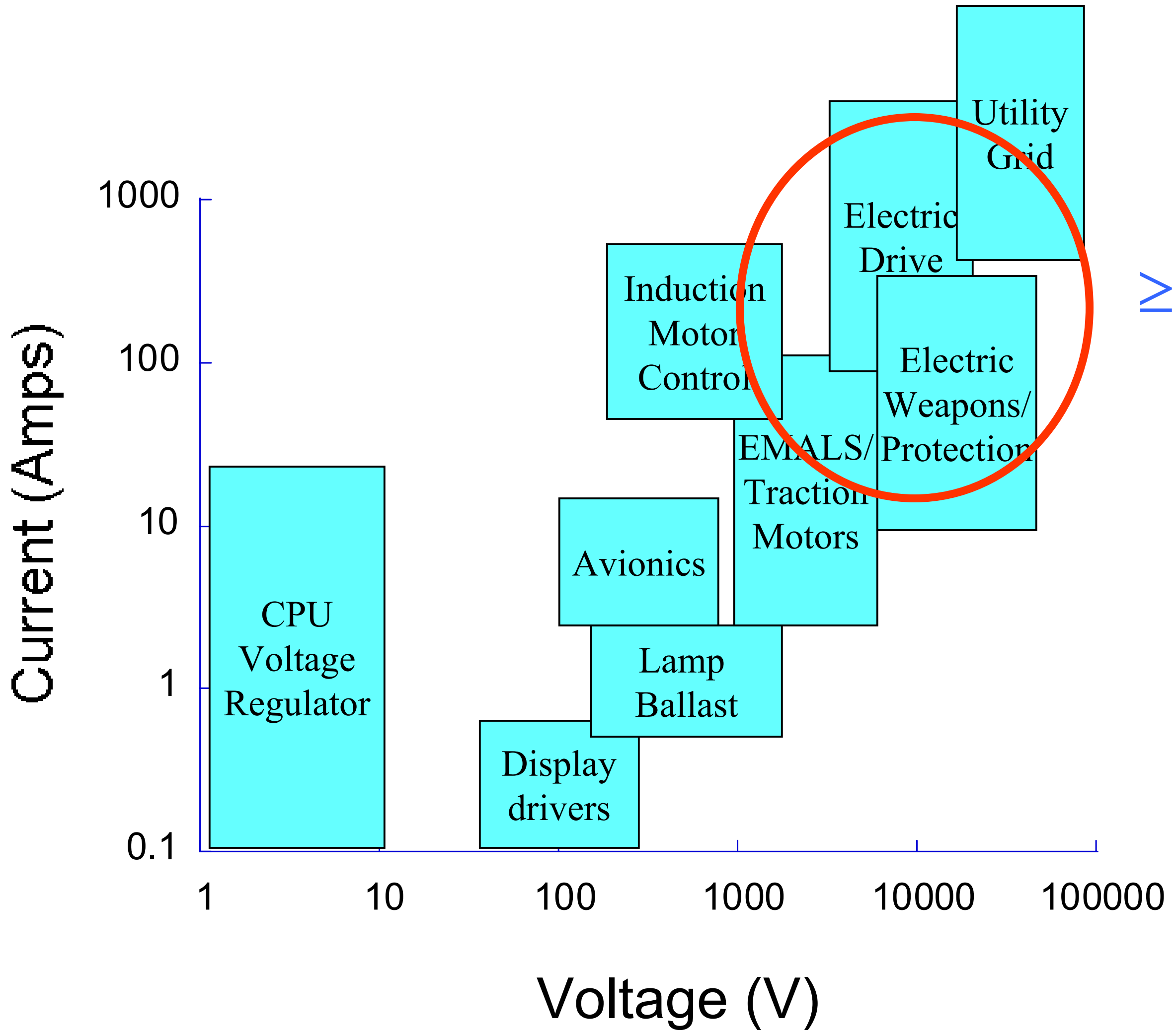


Simplified circuits and expanded capability

Smaller, lower loss, active and passive components

Smaller cooling systems

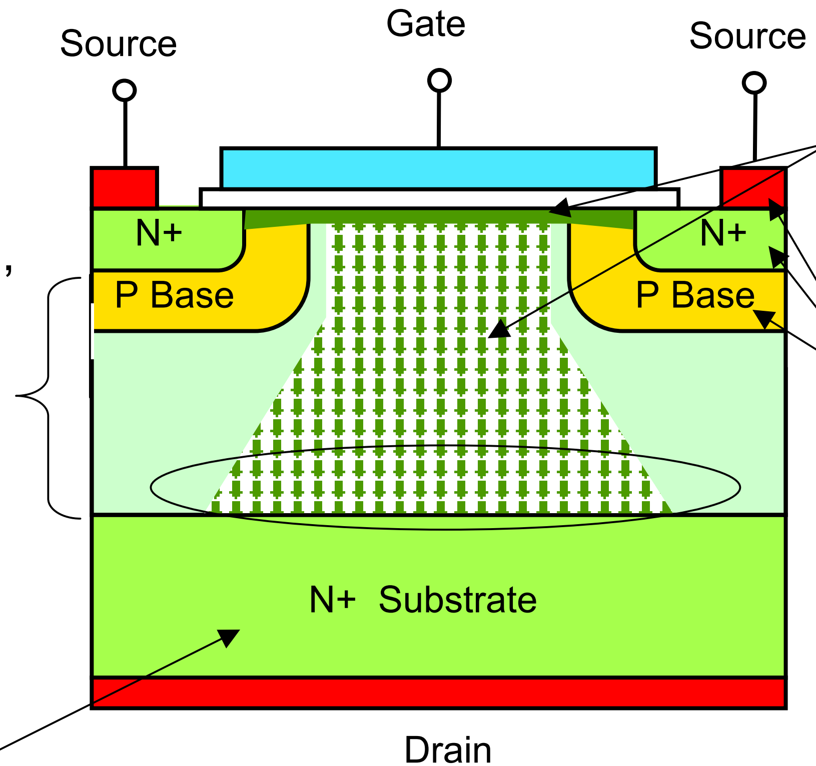
Power Electronics Applications



HPE Target:
≥ 10 kV ≥ 100 A

Technical Challenges

Thick, lightly doped, low defect density, epitaxial layer (150 μm, <1.5 defects/cm^2, 5% uniformity)



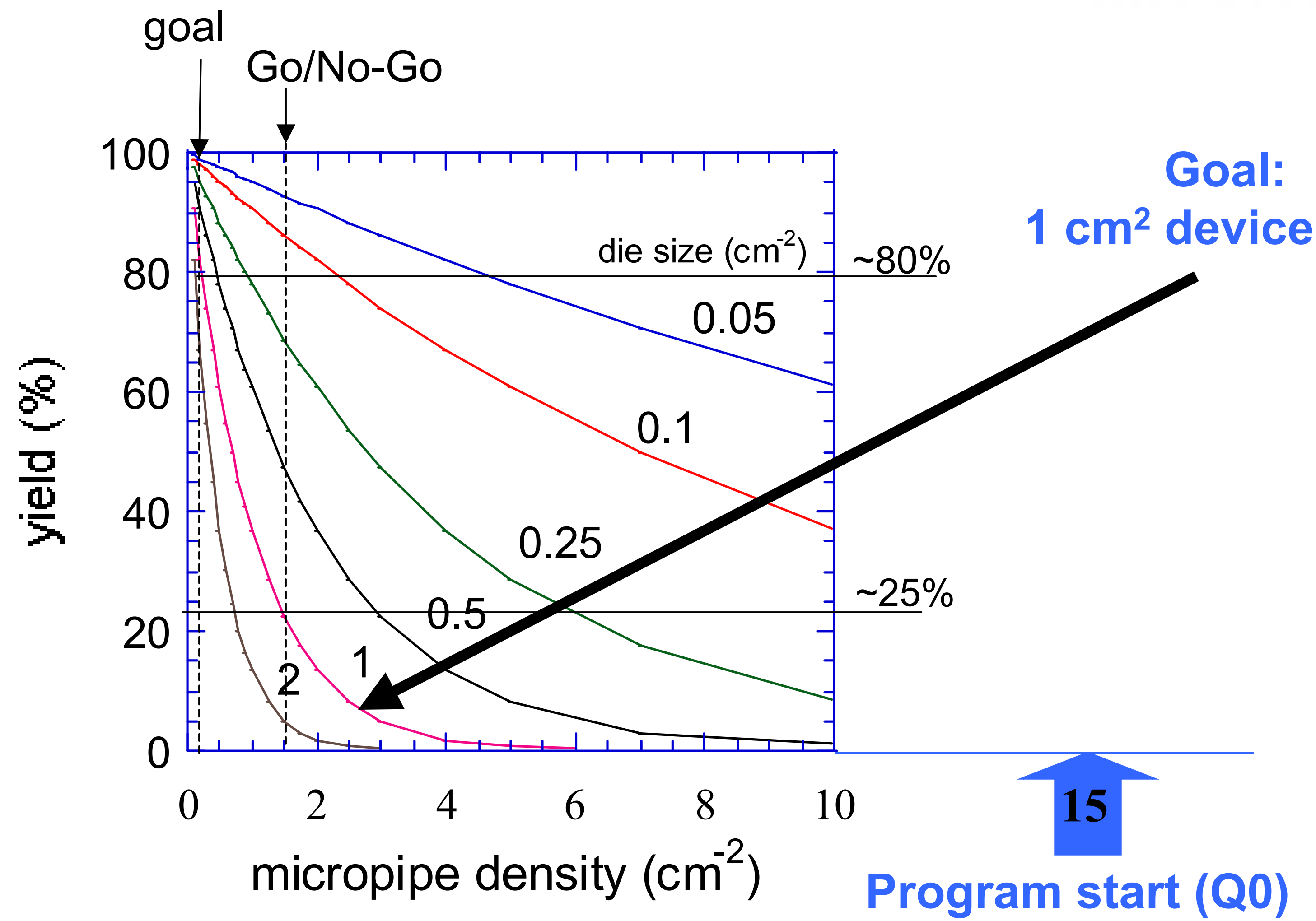
Low on-state resistance (R_{on} <0.25 Ω-cm^2; V_f < 4.5 V)

Process Technology (MOS: μ>100 cm^2/Vs, contacts, implantation)

Large defect-free substrates (<1.0 micropipes/cm^2)

SiC Power Transistor

Material Quality Yield Limits



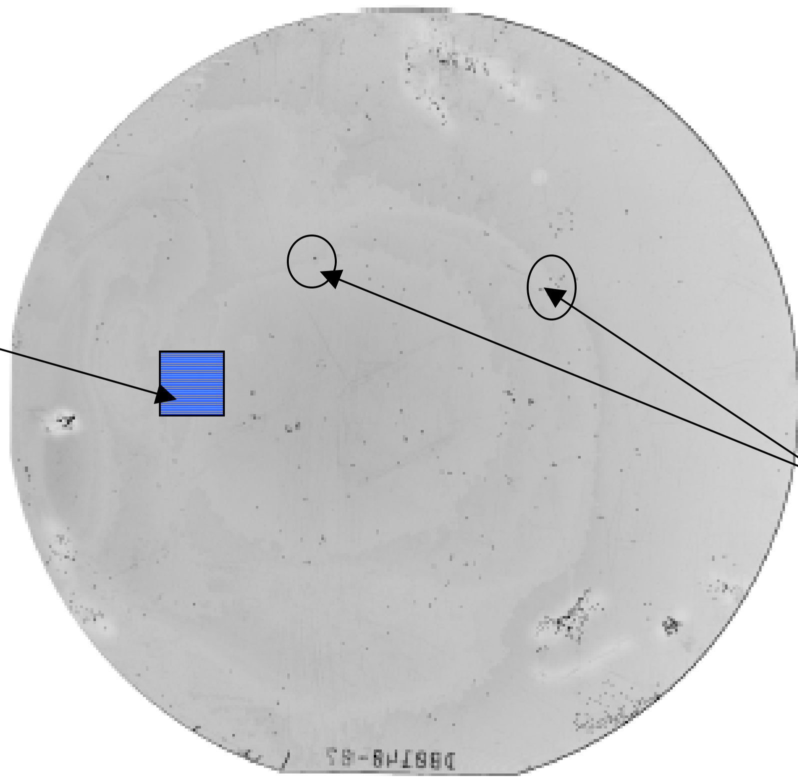
Dislocations: not catastrophic but degrade device performance

Material Quality for Large Area Devices

Status in May ‘02:

15 upipes/cm^2, dislocations > 10,000 cm^{-2}

~100 A power device

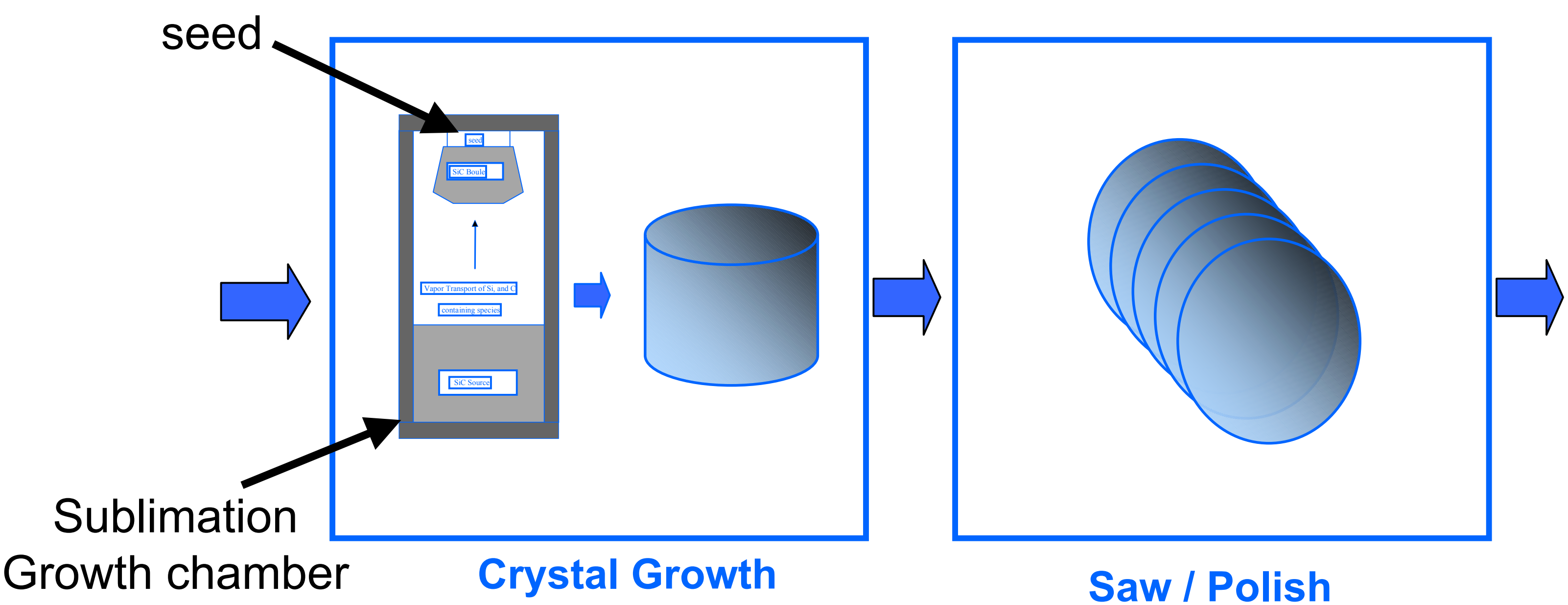


Micropipe: open core dislocation propagating through entire wafer that are catastrophic to device operation

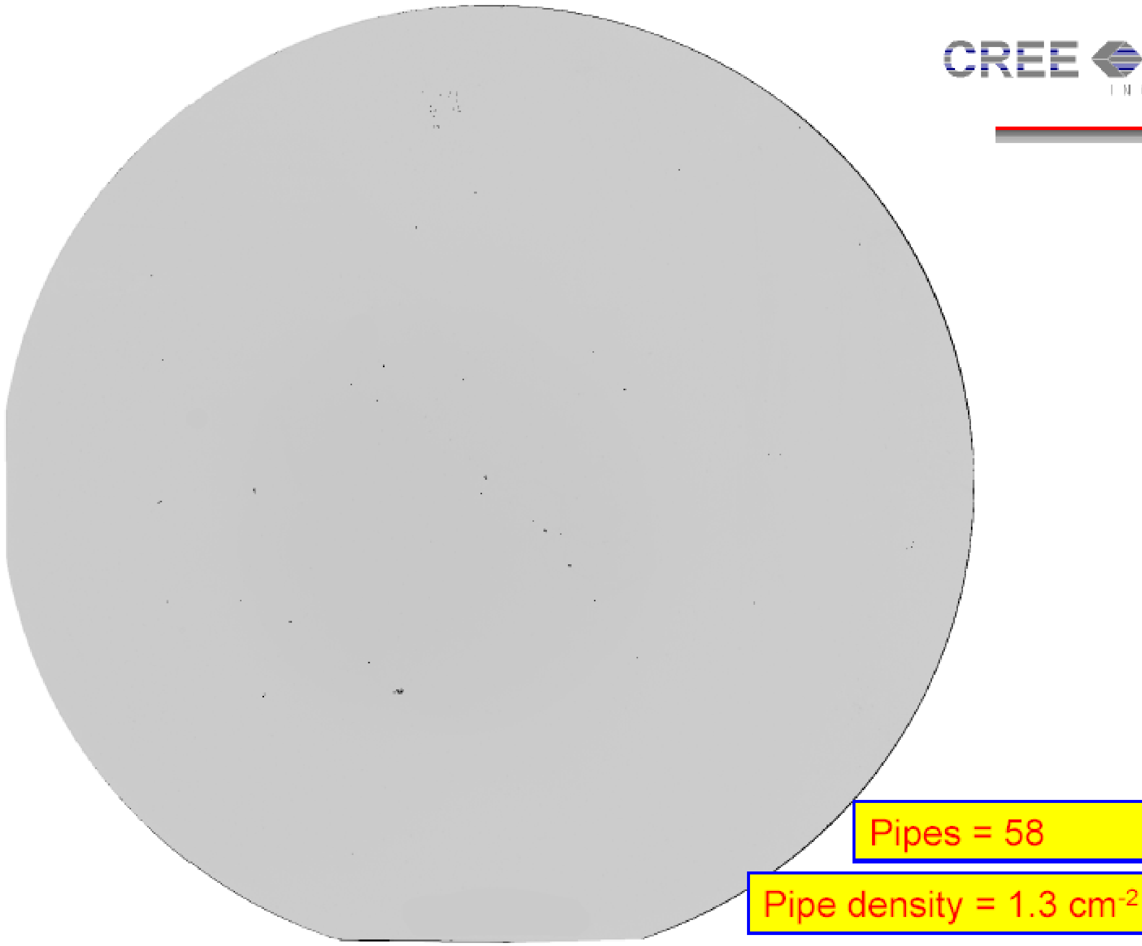
75 mm 4H SiC n-type wafer

Initial Cystal Growth Steps

- High quality, large area SiC seeds
- SiC wafering (saw, lap, and polish)



Metric 1: <1 upipe/cm^2 for 75 mm

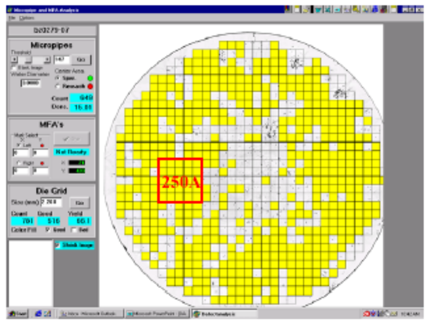


75 mm 4H SiC

Yield Estimate from Micropipe Density

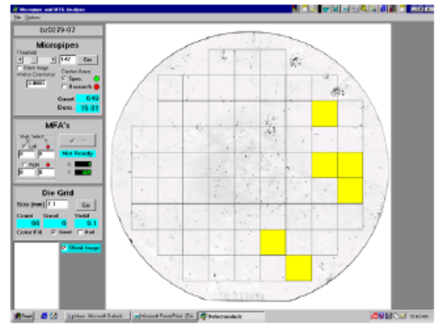
- For our kickoff meeting “good” 3” wafers, the expected yield of 10 and 100 A devices is shown below (Loss due to pipes only)

10 A device



Yield = 66%

100 A device

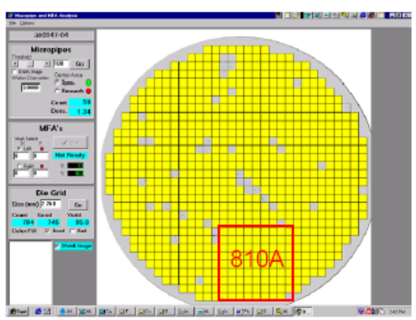


Yield = 9%

Pipe density = 15 cm^{-2}

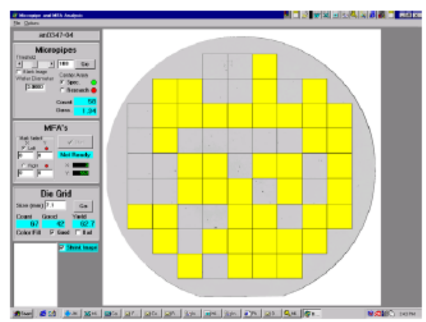
- For our current “good” 3” wafers the expected yield of 10 and 100 A devices is shown below (Loss due to pipes only)

10 A device



Yield = 95%

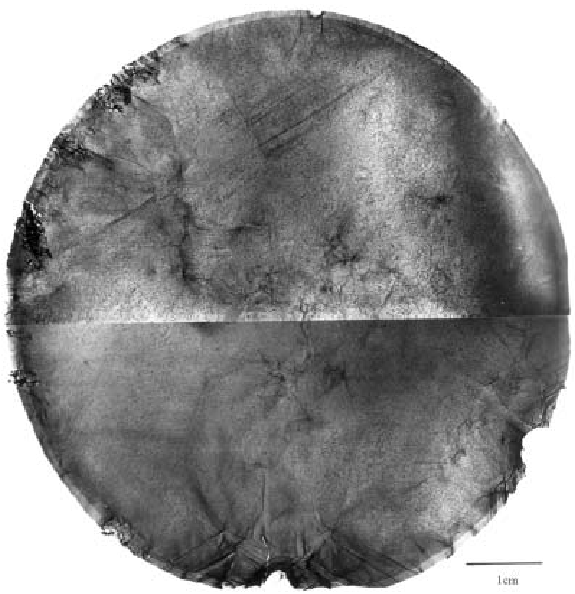
100 A device



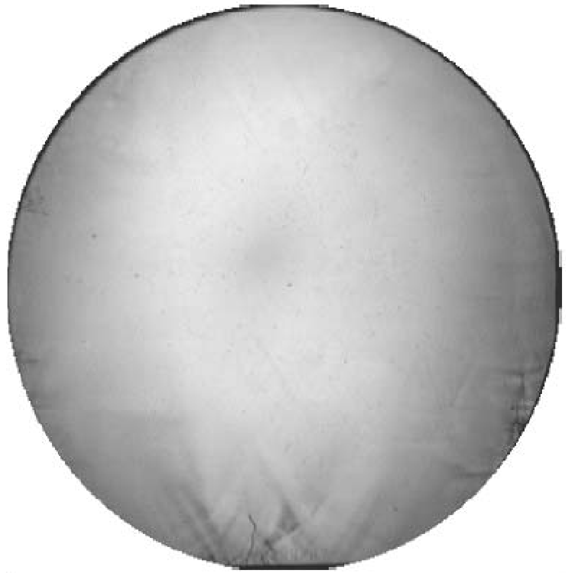
Yield = 62%

Pipe density = 1.3 cm^{-2}

Metric 2: <500 dislocations/cm^2

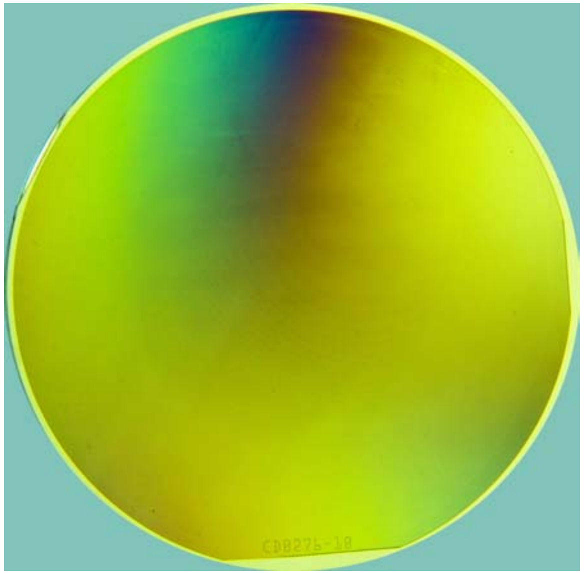


Back-reflection XRT



Cross polarizer Image

Cree

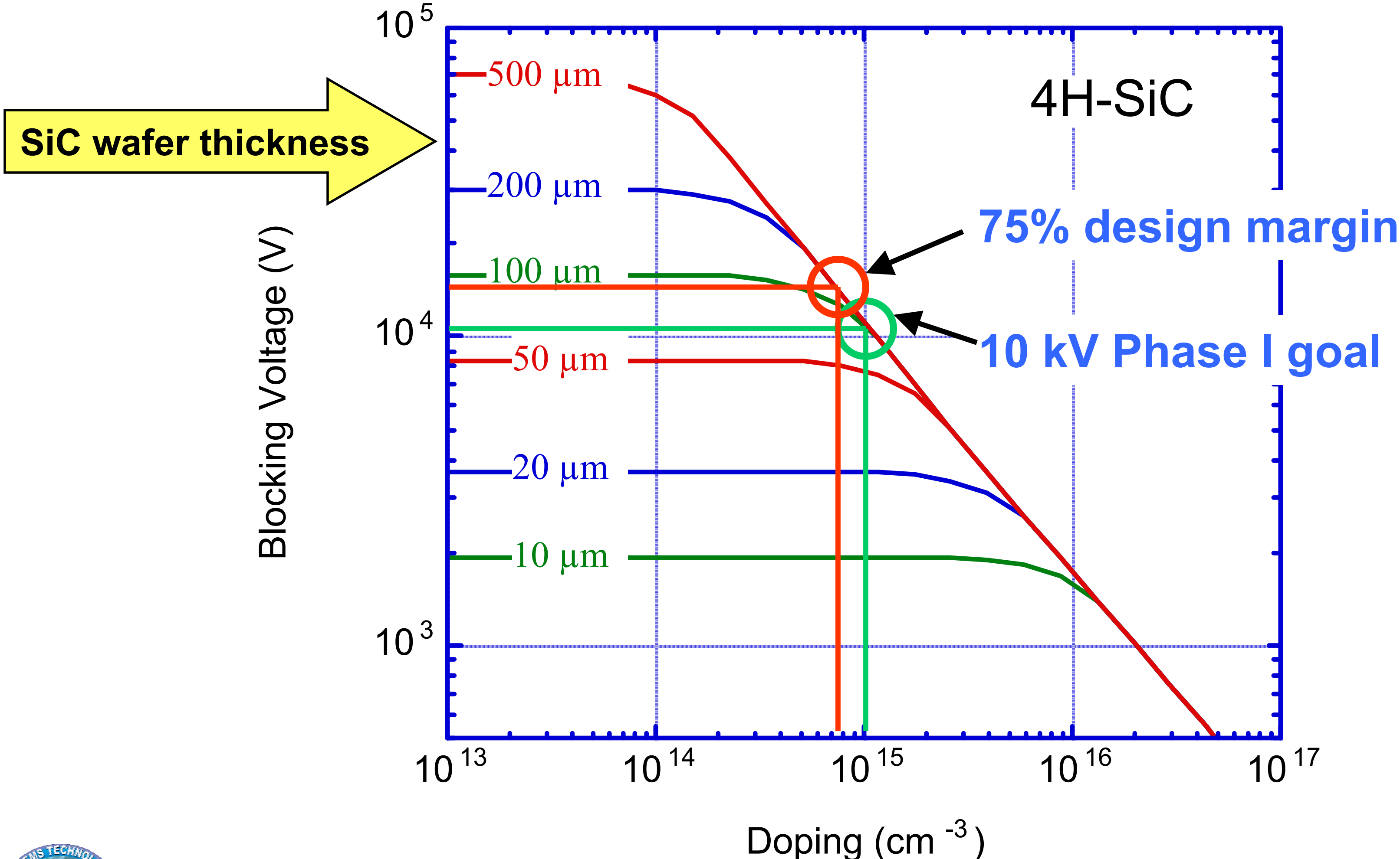


Tri-service image

$N_{dis} > 5000\ cm^{-2}$

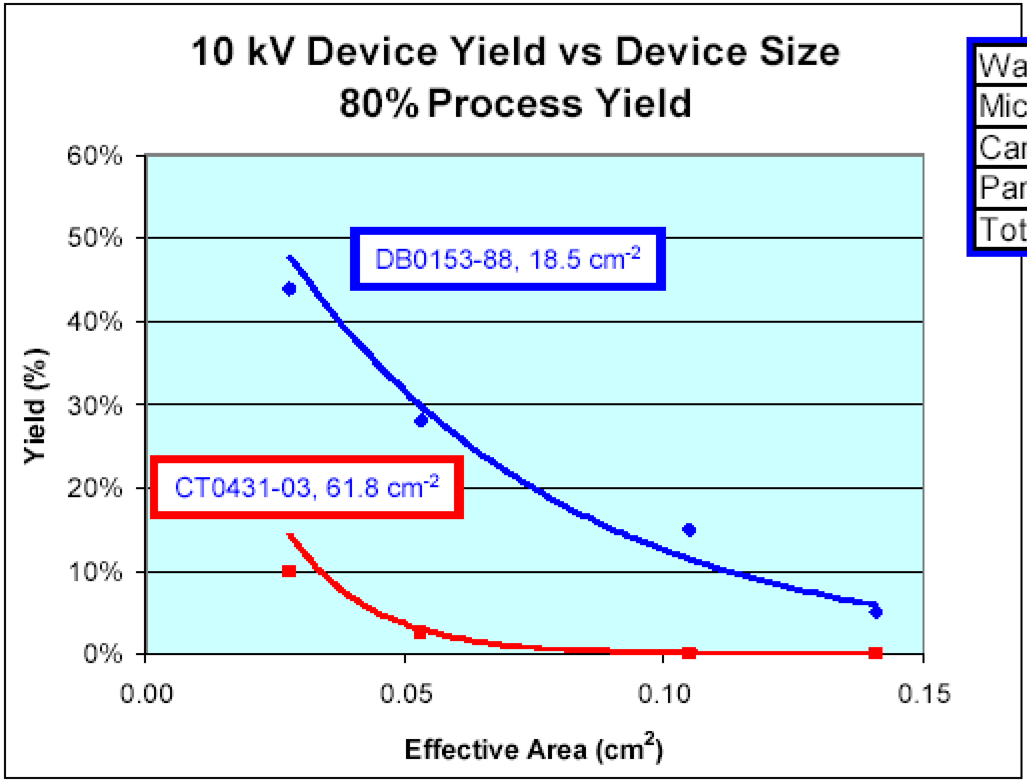
Reduced wafer stress required for dislocation reduction

10 kV SiC Epitaxy



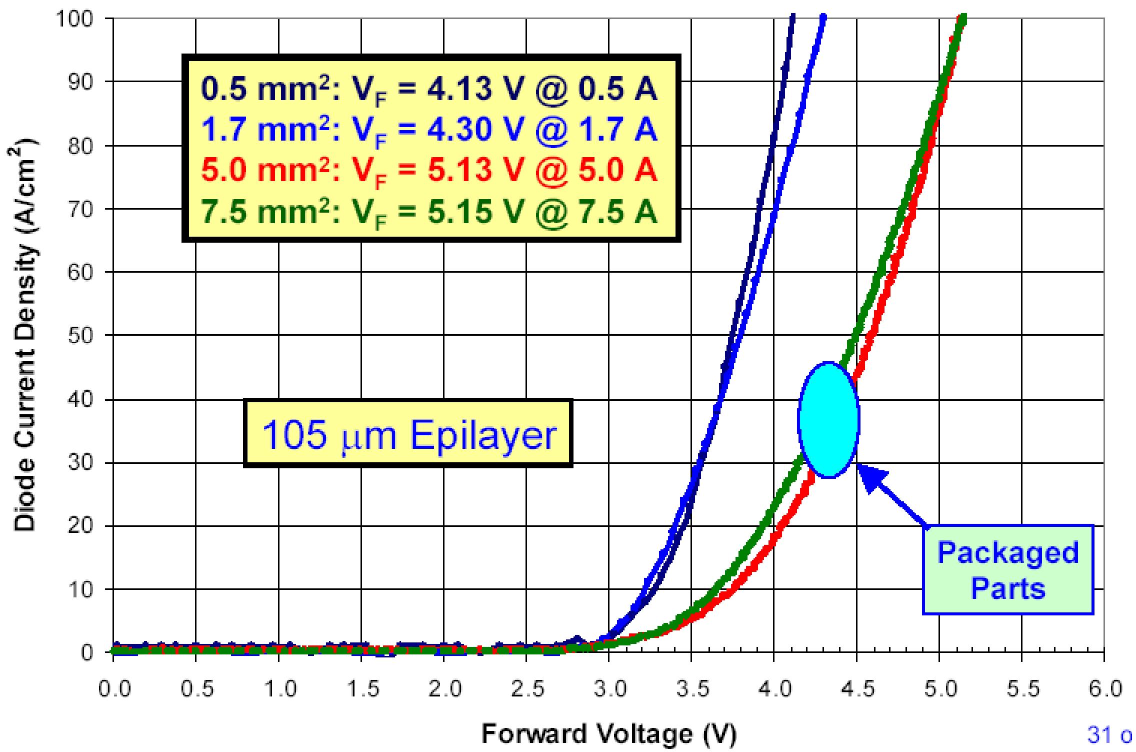
Metric 3: 100 μm epitaxy with <1.5 electrically active defects/cm^2

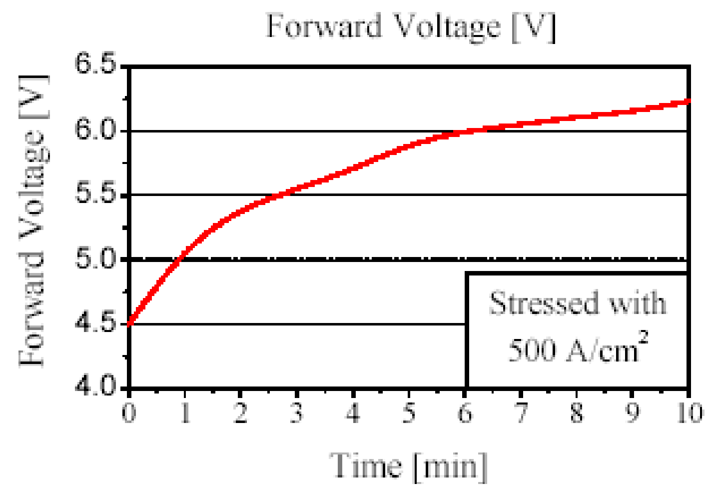
100 Micron Thick Epilayers Grown Using 3X3-inch Susceptor



Wafer =>	DB0153-88	CT0431-03
Micropipe	4.7	13.9
Carrots	1	1.5
Particles	2	2
Total:	7.7	17.4

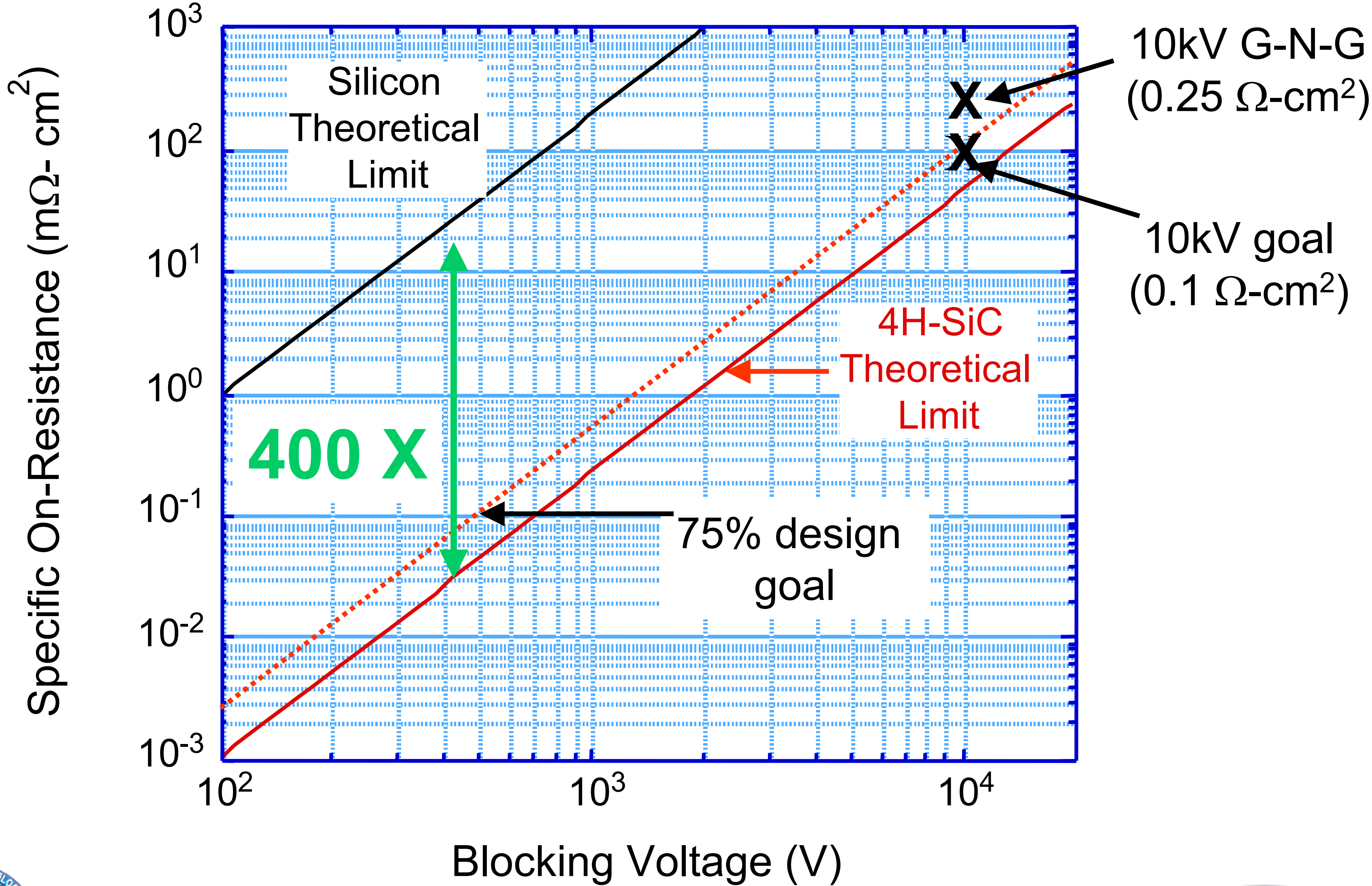
Metric 4: 10 kV PIN with $V_f < 4.5$ V at 100 A/cm^2



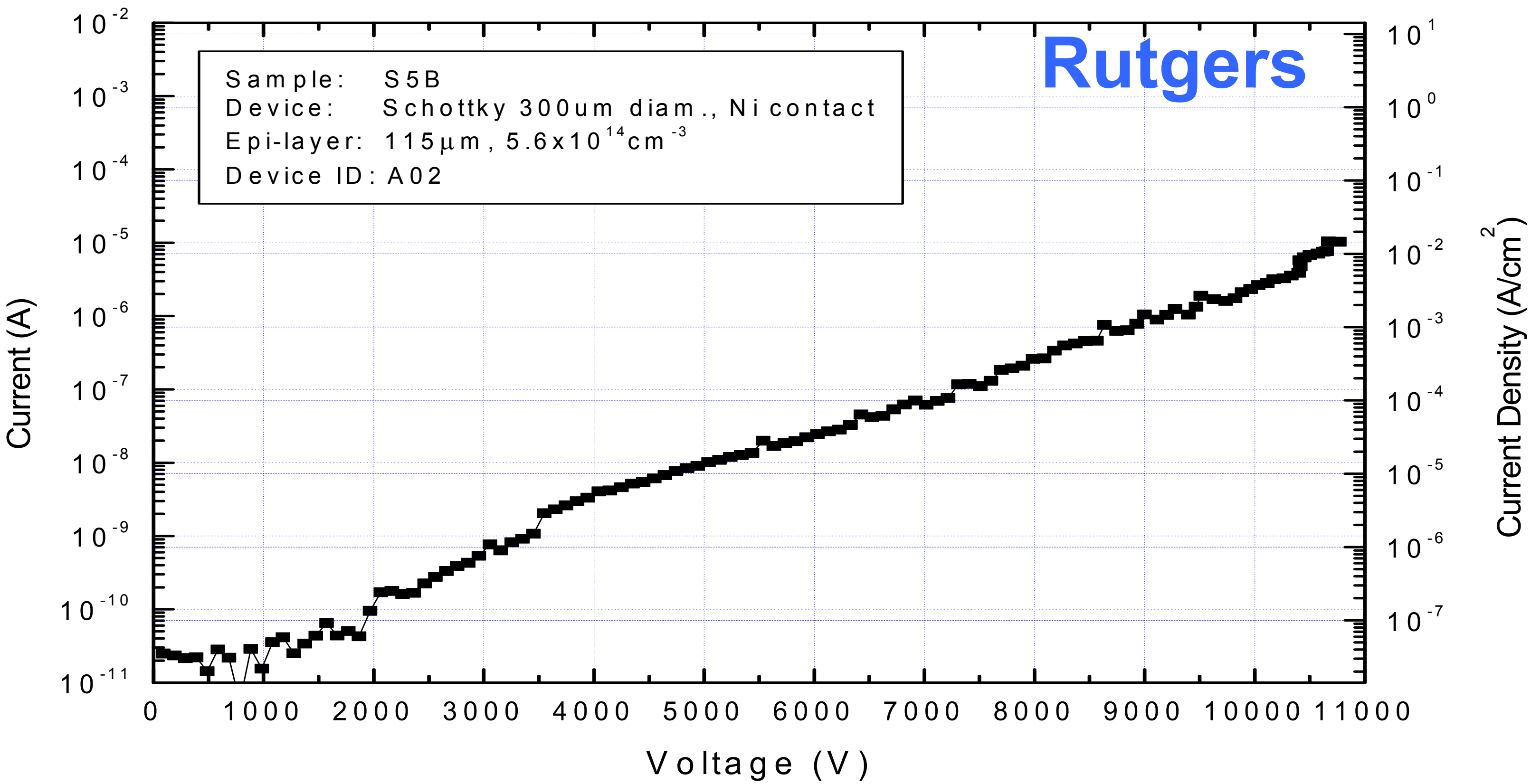


Encouraging initial V_f, but rapid degradation

On-state characteristics: FET



Metric 5: 10 kV unipolar on-state resistance < 0.25 Ω-cm²

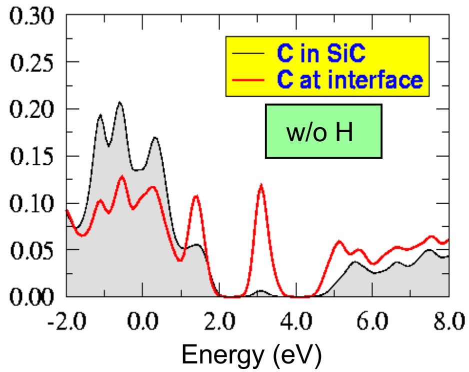


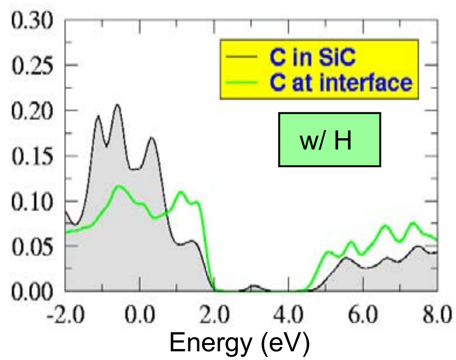
10,800V Schottky Barrier Diode

R_{sp_on}=159 mΩ-cm² , μ = 778 cm²/Vs

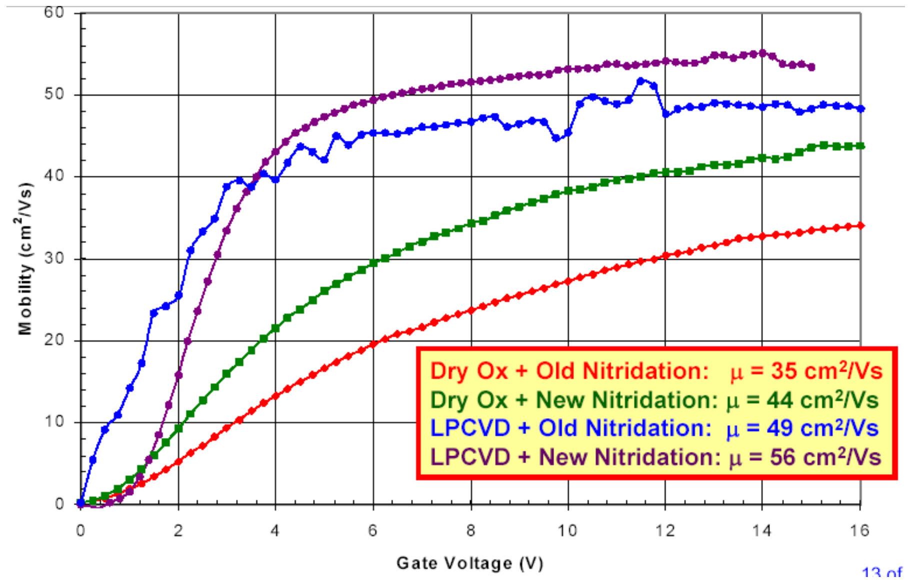
Metric 6: 100 cm^2/Vs inversion channel mobility

DFT Calculations





H passivates C dangling bonds, but not C band edge states.



Recent result: 72 cm^2/Vs

Improvements not yet demonstrated in implanted p-well

Performers: RF, HPE, RF&HPE

SiC Substrate Technology:

- Cree
- Sterling Semiconductors
- Carnegie Mellon University
- Penn State University

Alternate Substrates

- ATMI
- Crystal IS

Processsing/Material Validation

- RCS
- Purdue
- RPI
- Rutgers

Epitaxial Technologies

- Cree/Cree Lighting
- ATMI
- Emcore
- Raytheon
- HRL
- Northrop Grumman (TRW)
- UC –Santa Barbara
- University of Texas
- University of South Carolina
- Sterling
- Georgia Tech

Assesment and Validation

- Government Evaluation Team

HPE Milestones and Status

task	Program start	Current status	12-18M	Goal
1. SiC substrate	**15 for 3 inch**	**1.3 upipes/cm^2 demo'ed**	**(a) < 1 micropipes/cm^2 for 3 inch** ; (b) **< 10 micropipe/cm^2 for 4 inch**	**(a) < 0.2 micropipes/cm^2 for 3 inch** ; (b) **< 1.0 micropipes/cm^2 for 4 inch**
2. SiC substrate	**>10,000 for 3 inch**	**Reduced stress, dislocation counting initiated, counts >> 500**	**(a) < 500 dislocations/cm^2 for 3 inch** ; (b) **< 1000 dislocations/cm^2 for 4 inch**	**(a) < 50 dislocations/cm^2 for 3 inch** ; (b) **< 100 dislocations/cm^2 for 4 inch**
3. Thick epitaxy	**50 um available, doping spec +/- 50%, defects not quantified**	**100 u epi demo'ed with 1.8% σ/mean; defects being identifies and reduced understood, ~4/cm^2**	**100 um epi with < 5% thickness and doping variation at 5x10^{14}cm^{-3} with < 1.5 total electrically active defects/cm^2 on 3 inch;**	**150 um epi with < 5% thickness and doping variation at 1x10^{14}cm^{-3} with < 0.5 total electrically active defects/cm^2 on 3 inch** ;

Red = primary milestones

On track (yellow) **Major challenges** (red)

HPE Milestones and Status-2

task	Program start	Current status	12-18M	Goal
4. PIN on-state	V_f > 6V (pulsed) with large forward drift	V_f < 4.5 V demo'ed for 1.7 mm² die, rapid degradation	10 kV, PIN with V_f < 4.5 V at 100 A/cm² (≥ 50 A total current) with <100 mV drift over 100 hours	10 kV, PIN with V^f ≤ 3.5 V at 100 A/cm2 (≥ 50 A total current) with <100 mV drift over 100 hours
5. FET on-state	Not demonstrated for 10 kV	Demo's of < .2 Ω-cm² for 10 kV	0.25 ohm-cm² with 10 kV blocking	0.10 ohms-cm² with 10 kV blocking
6. mobility	<25 cm²/Vs	72 cm²/Vs for p-epi; no result on implanted p-well	100 cm²/V-s in implanted p-well	200 cm²/V-s in implanted p-well

On track (yellow) | Major challenges (red)

Red = primary milestones

Status Summary

- Wide bandgap semiconductor (SiC) high power electronics is a critical enabler for future DoD systems
- DARPA's HPE program status:
  - On-track:
    - Substrate micropipe demonstration
    - Thick Low Defect Epitaxy
    - FET on-state resistance
  - Major challenges remain
    - Dislocation reduction
    - PIN V_f drift
    - Inversion channel mobility in implanted p-well
- Commercial SiC power products exist and are poised to impact new applications
- Technology is on the verge of a revolution in power electronics based on SiC technology

Projection

- Full exploitation of emerging SiC power technology will require new systems implementations

- Integrated control and dynamic “smart” power will increase platform capability and survivability

END