

Development of High Data Rate VCSELs

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C2OI Kickoff

Chantilly, VA

June 23, 2003

This work is supported by DARPA through contract DAAD 19-03-1-0059.

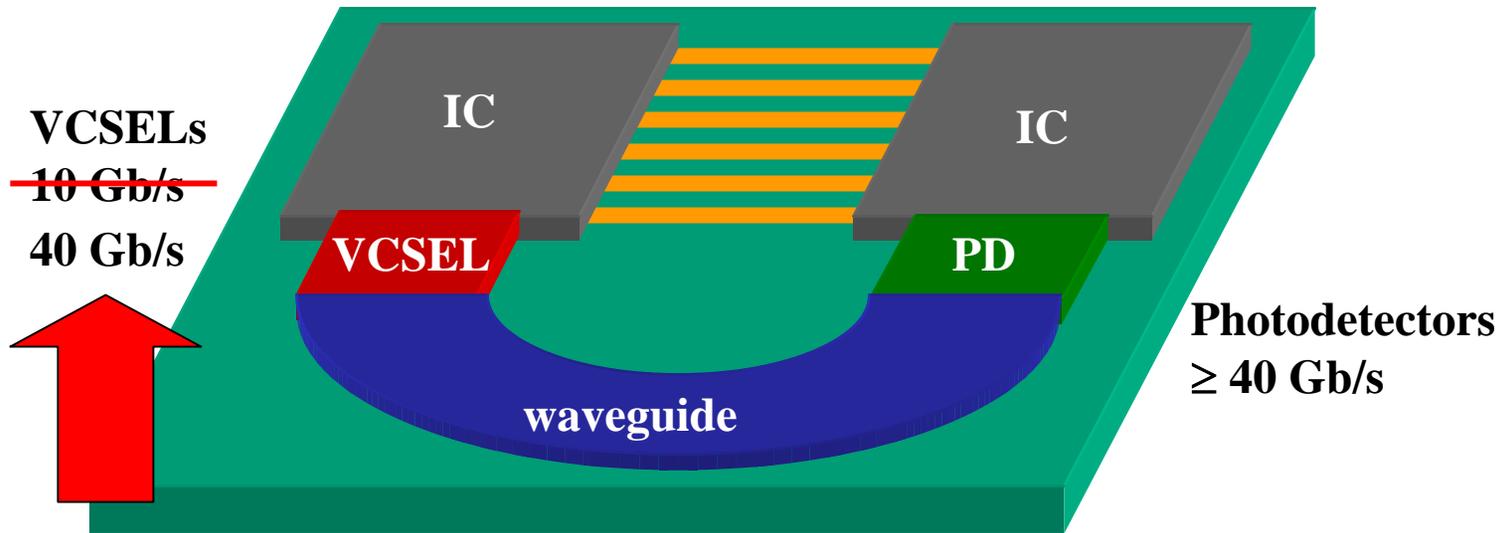
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Outline

- Background
 - Motivation
 - State of the Art
- Limitations/Approach
 - Circuit
 - Resonance Frequency
 - Saturation Current
- Programmatic
 - Roadmap
 - Goals
- Opportunities for Collaboration

C2OI Components

Electrical interconnects 5Gb/s → 10 Gb/s



VCSELs
~~10 Gb/s~~
40 Gb/s

Photodetectors
 ≥ 40 Gb/s

Waveguides
 $\sim 5-10$ Tb/s-cm

High Speed VCSEL State of the Art

➤ Data Rates

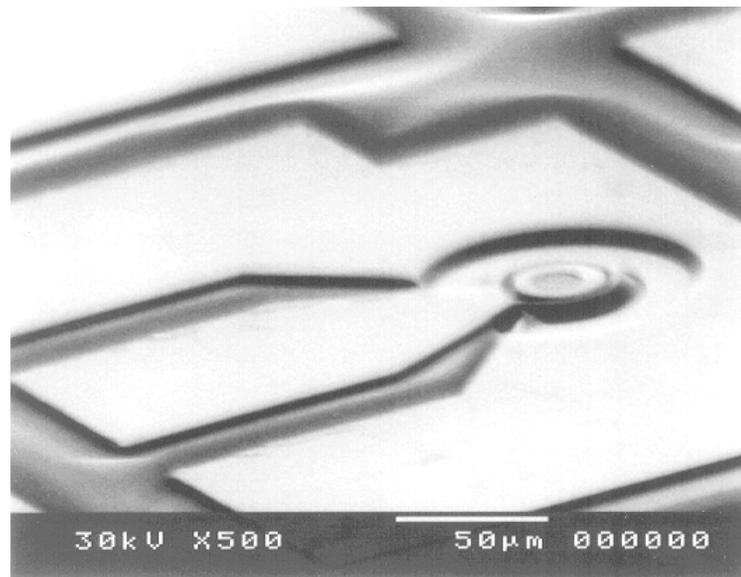
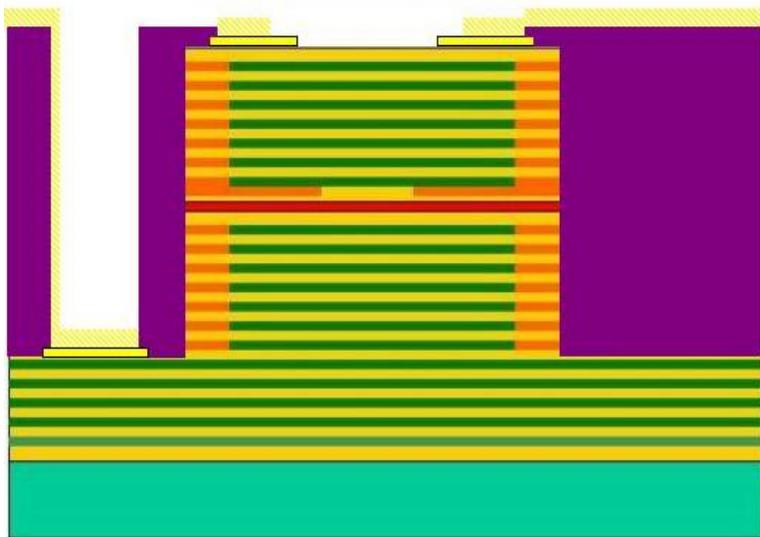
- Commercial: 10 Gb/s available
- Published Research: ~12 Gb/s
 - Lear et al, *Trends in Optics and Photonics Series*, 15, 69 (1997)
 - Michalzik et al, *IEICE Trans. on Electron.* E84C, 629 (2001)

➤ “Small” Signal Modulation Bandwidths

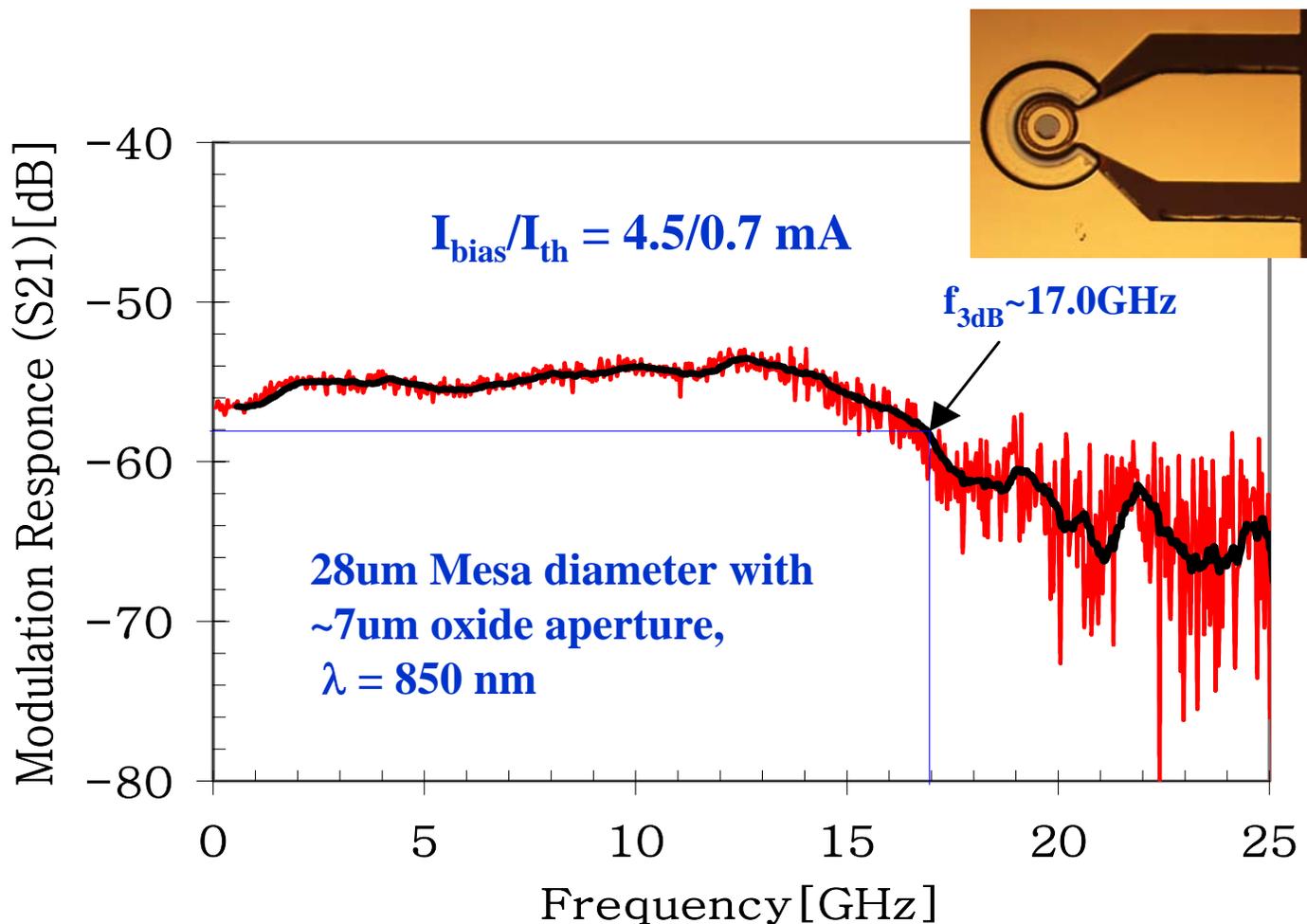
- Commercial: ~8 GHz
- ~15 GHz for proton implanted
 - Shtengel et al, *Photon. Tech. Lett.*, 5, 1359 (1993);
 - Satuby et al, *Photon. Tech. Lett.*, 10, (1998)
- ~16 GHz for oxide confined
 - Lear et al, *Electronics Letters*, 32, 457, (1996)
 - Thibeault et al, *Photon. Tech. Lett.*, 9, 11 (1997)
- ~21 GHz for oxide confined with implant
 - Lear et al, *Trends in Optics and Photonics Series*, 15, 69 (1997)

VCSEL Fabrication at CSU

- Oxide confined
 - high photon density
- Polyimide planarization
 - simple capacitance reduction
 - issues on metal adhesion
- Top emitting, $\lambda=850$ nm
- Coplanar waveguide pads
 - May adapt for packaging



CSU High Speed VCSELs – Results

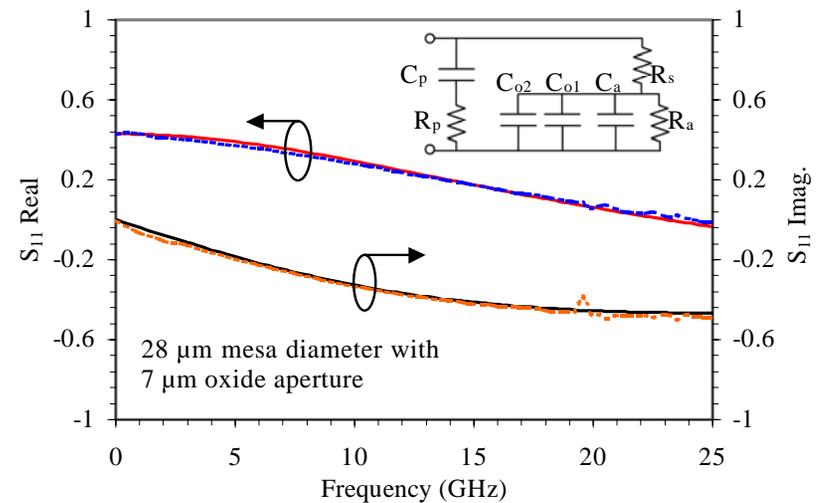
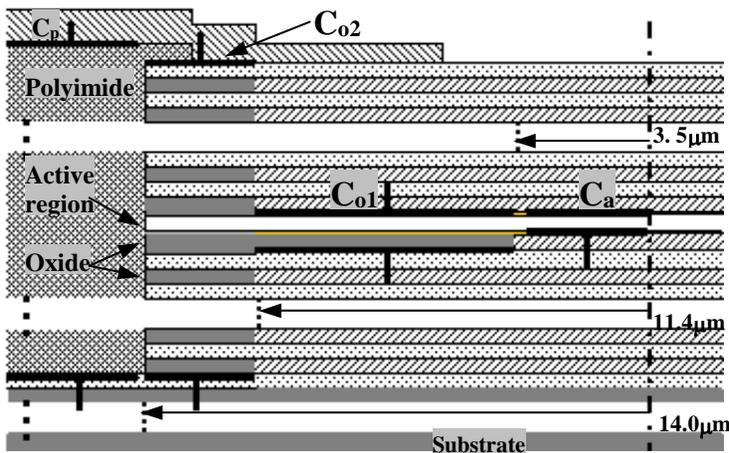


Limitations to VCSEL Bandwidth

- Electrical -- parasitic circuit elements (RC, no package L)
- Resonant frequency -- $f_{3\text{dB}} = 1.55f_0 (I/I_{\text{th}} - 1)^{1/2}$ until
 - Mode competition
 - Heating
 - Damping
 - Non-linear gain saturation
- Want high f_0
 - 850 nm devices with 10 GHz/ $\sqrt{\text{mA}}$ and $I_{\text{th}}=0.5 \text{ mA} \rightarrow f_0 \sim 7 \text{ GHz}$
- Want high $I_{\text{max}}/I_{\text{th}}$
 - Thermal dissipation
 - Reliability degradation

Mesa Capacitance Reduction

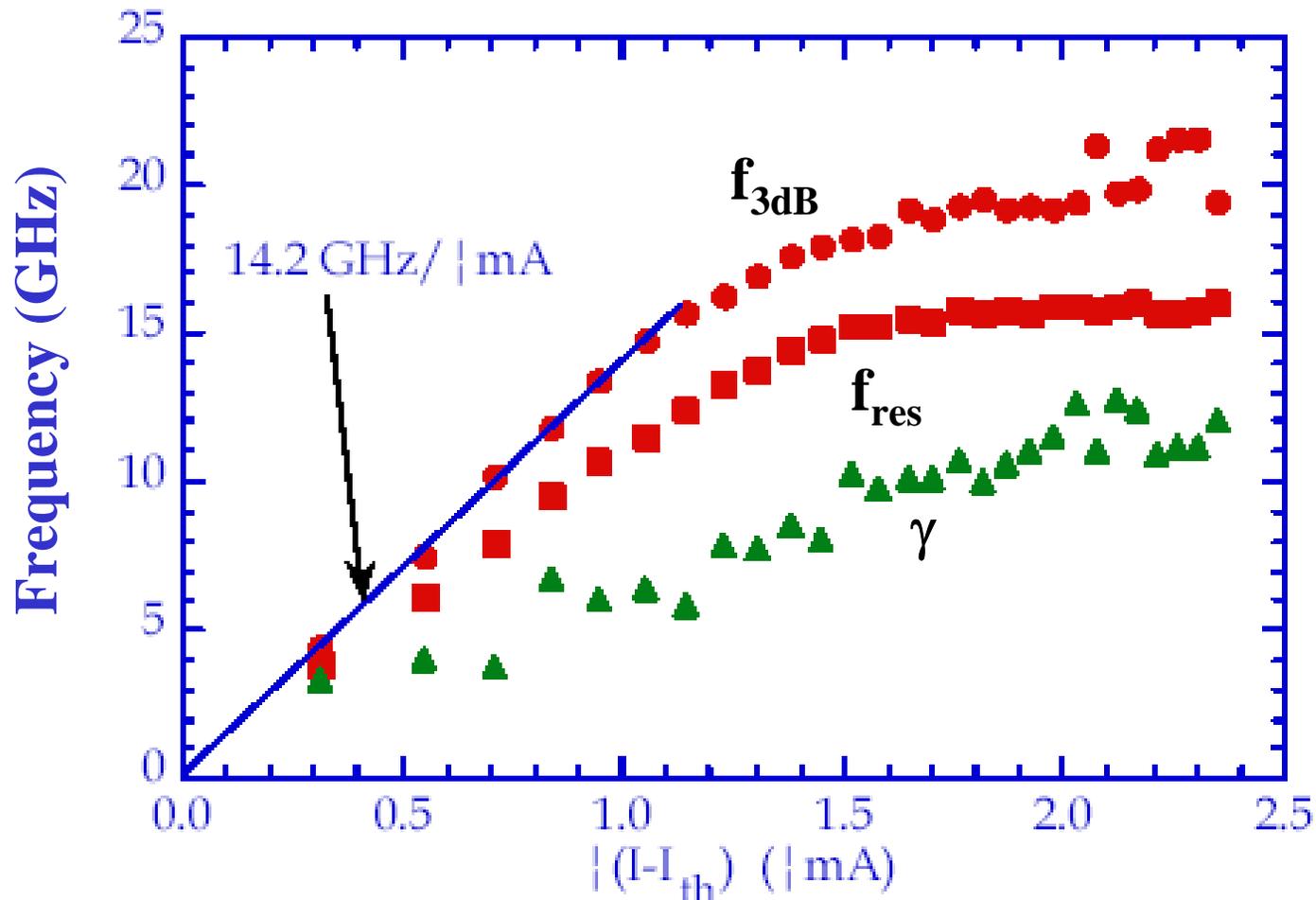
- Smaller mesas → lower mesa capacitance
 - ~150 fF without implantation
- Use S_{11} network analyzer data to extract circuit parameters
- Electrical circuit 3dB bandwidth is ~30 GHz
- Neglected diffusion capacitance in modeling



Optimizing the Resonance Frequency

- Want resonance frequency to increase rapidly with increasing current bias, $f_{\text{res}} = f_0 (I/I_{\text{th}} - 1)^{1/2}$
- $2\pi f_0 = [\tau_{\text{carr}} \tau_{\text{phot}}]^{-1/2} \propto (\partial g/\partial n)^{1/2}$
- Want high differential gain
 - GaAs QW $\partial g/\partial n = 0.77 \times 10^{-15} \text{ cm}^2$, expt. $f_0 = 7 \text{ GHz}$
 - InGaAs QW $\partial g/\partial n = 1.13 \times 10^{-15} \text{ cm}^2$, expect $f_0 = 8.5 \text{ GHz}$
 - S. Weisser et al, *Photon. Technol. Lett.*, 8, 608 (1996) reports $\text{In}_{0.35}\text{Ga}_{0.65}\text{As}$ QW $\partial g/\partial n = 2.2 \times 10^{-15} \text{ cm}^2$, used to achieve 40 GHz edge-emitting laser diodes
- Need sufficiently low damping to reach high f_{res}
 - Analysis of 850 nm VCSELs predicts $f_{\text{res,max}} = 58 \text{ GHz}$

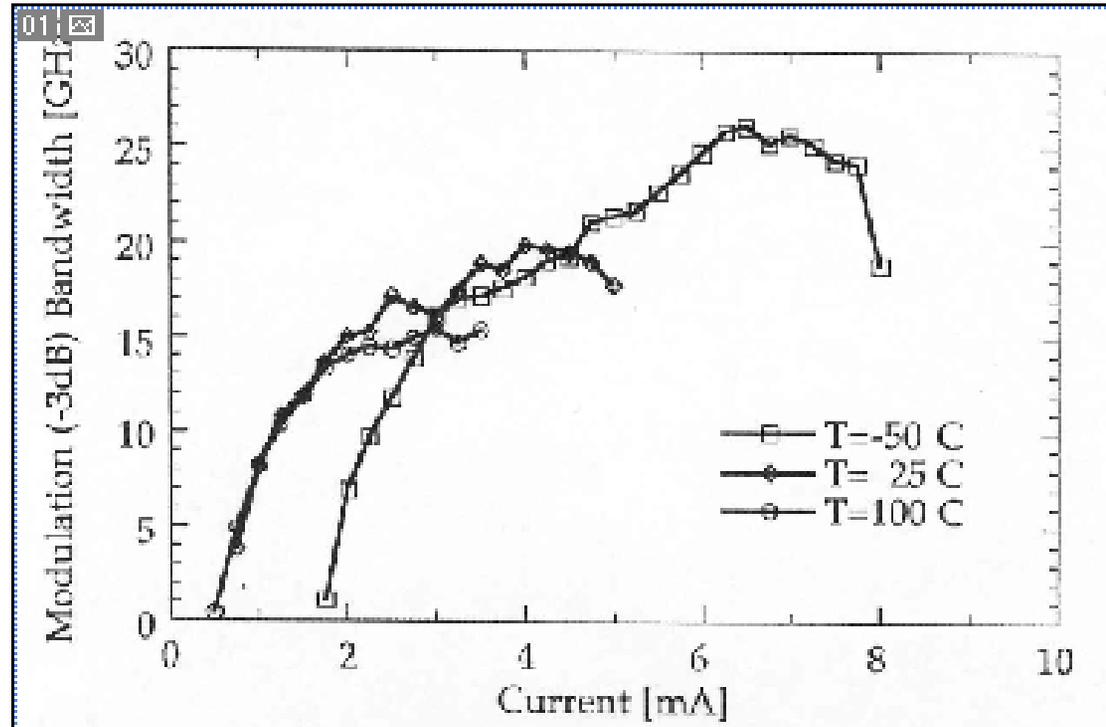
Resonant Frequency & Damping vs. I



$K=0.159$ and $\gamma_0=18.8/\text{ns}$ \rightarrow intrinsic 3dB bandwidth of 58 GHz.

Limits to High Current Operation

- Mode control – spatial hole burning
 - Issues with coherence in MMWG
- Thermal management



Roadmap to Higher Speed VCSELs

Data Rate [Gb/s]	Milestone Date	f_{res} [GHz]	I/I_{th} (GaAs)	I/I_{th} (InGaAs)	P_{elec} [mW] (InGaAs)	$R_{\text{th,max}}$ [C/mW]
20	4/04	10.3	3.2	2.5	1.7	18.2
30	4/05	15.5	5.9	4.3	3.2	9.8
40	4/06	20.7	9.7	6.9	5.6	5.6

➤ Assumptions:

$$I_{\text{th}} = 0.5 \text{ mA}, R = 100 \text{ } \Omega, \Delta T_{\text{max}} = 25\text{C}$$

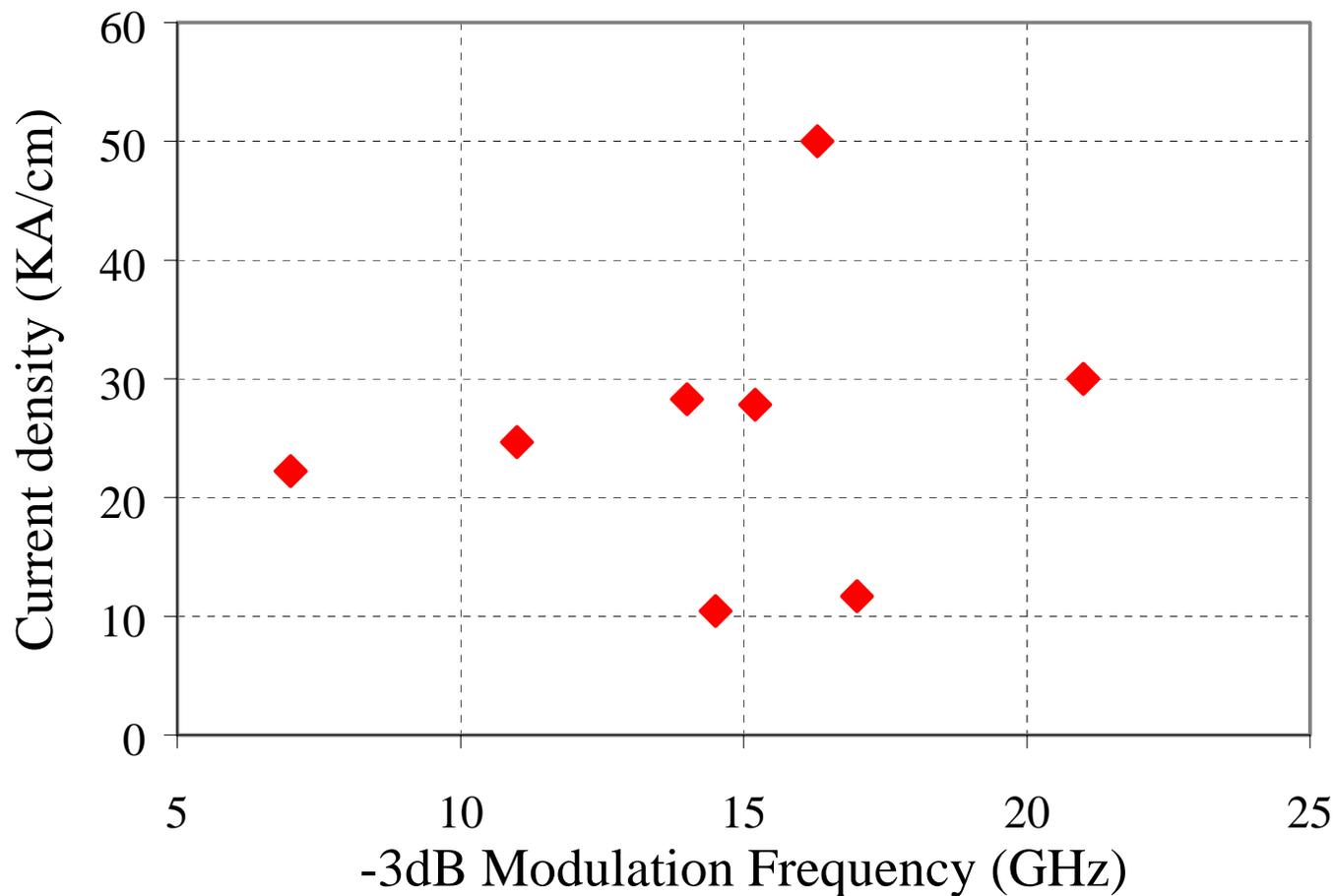
Program Goals

- #1: Demonstrate a 10 Gb/s increase each year
- #2: Develop fabrication/packaging approaches to maximize VCSEL data rates
- #3: Insert high speed VCSEL technology into larger C2OI program
- #4: Model phenomena that could limit modulation bandwidth

Systems Issues for VCSEL Insertion

- SM VCSEL coherence in MM waveguide
- $\lambda=850$ vs. 980 nm compatibility with detectors, waveguide absorption
- Large signal modulation – extinction ratio
 - Separate effort in developing large signal models
- Operating temperature range
- Reliability at high current densities

Bias Current Density at High BW



Opportunities for Collaboration

- Systems issues
- Fabricate VCSELs for C2OI teams
 - Discuss details on resources, process limitations, epi ...
- Would welcome VCSEL epitaxy
- Need access to high data rate (≥ 20 Gb/s) BERT
- Could benefit from packaging expertise

Summary

- VCSEL speed needs to catch up with rest of C2OI
- Will address multiple aspects limiting speed
 - circuit, differential gain, modes, thermal
- +10 Gb/s per year
- Modeling and structure development
- Professor + students with VCSELs seeking relationship with C2OI partners for 3 years, maybe more.