IBM Milestones and Experience

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Agilent Technologies

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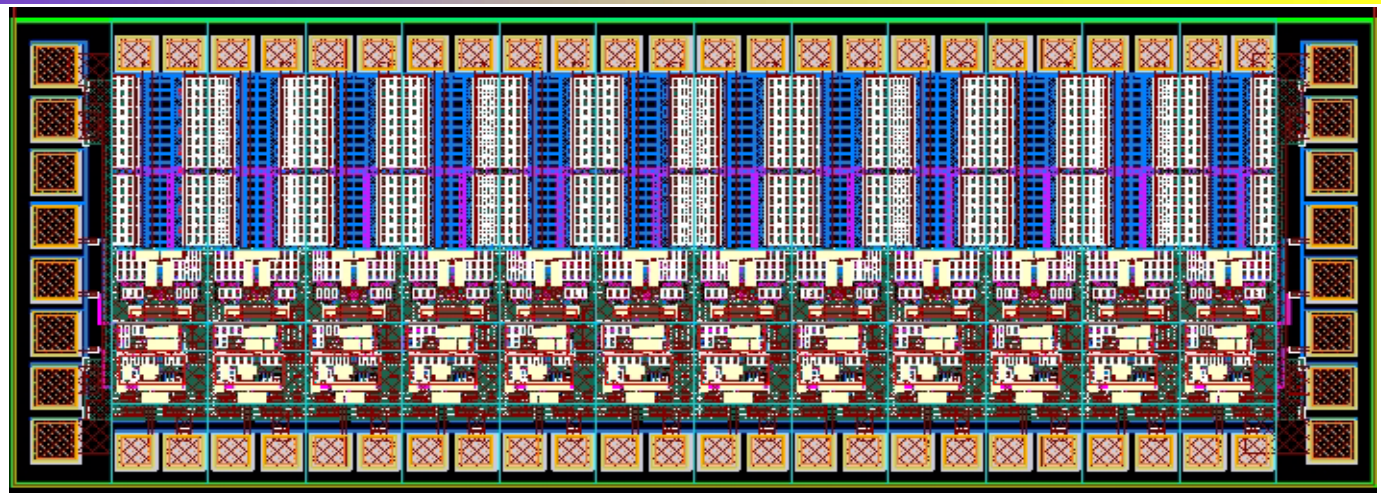
IBM Responsibilities

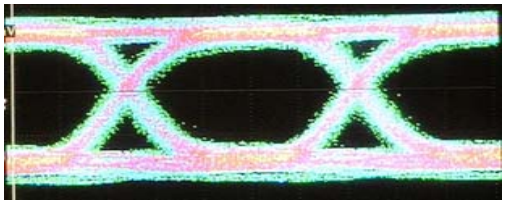
IC Chips
- Support to OE devices
- Interfaces to System

- Si Carrier (OPTOCHIP)
  - Optical and Electrical High density/high speed
- SLC Card (OPTOCARD)
  - Optical waveguides
  - High speed, high density electrical
- Assembly processes
- Optical Bus Design and Test
  - Optical Link Budget and Simulation
  - Parallel Link Test and Validation
- Lab Demo at up to 15 Gb/s per channel
- System Demo at < 10 Gb/s per channel

High speed IC Design, Fab, and Test



- Array of twelve 10 Gb/s VCSEL drivers, 100 mW each; 1.3 x 3.5 mm
- GOAL: Lowest-power and cost 10Gb/s VCSEL driver array for parallel links
  - Single 3.3V supply, 100mW / channel including VCSEL power
  - Single-ended and differential input designs
  - Limiting amplifier for input signal conditioning
  - Single-ended output to VCSELs (array is common cathode)
  - Adjustable VCSEL bias and modulation
  - Temperature compensation circuits for each driver in array



DifferentialOutput eye diagram at 10Gbit/sec

High speed IC Design, Fab, and Test

- Other IC designs
  - Analog SiGe and CMOS designs
  - Parallel TIAs and Limiting Amps
  - MUX and DeMUX, Clock and Data Recovery up to 40Gbit/sec

  - Extensive experience in high speed, low power designs

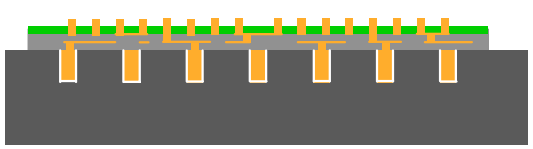
Si Carrier Processing Experience

Process Flow for Si Carrier with Through Vias

Etch vias into a bare Si wafer, oxidize for isolation

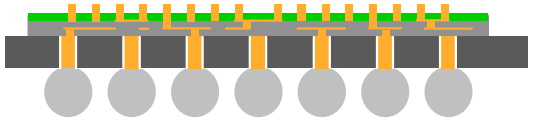
Fill vias with a conductor

Build wiring levels on carrier wafer frontside, including joining lands or bumps

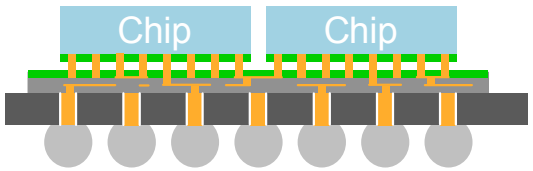


Thin wafer from the back to expose the filled vias

Build C4s on backside, dice wafer into carriers

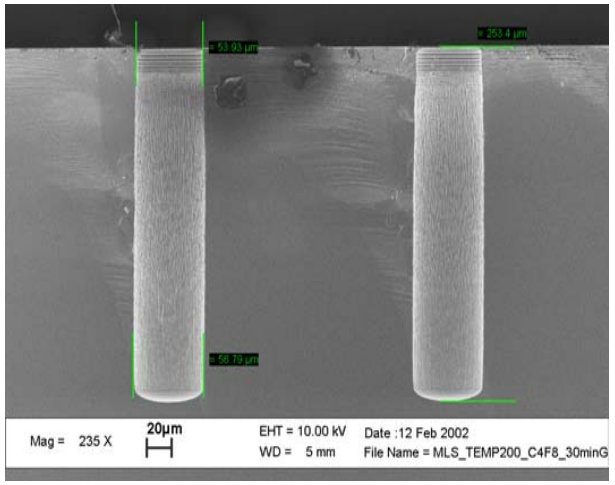


Attach chips

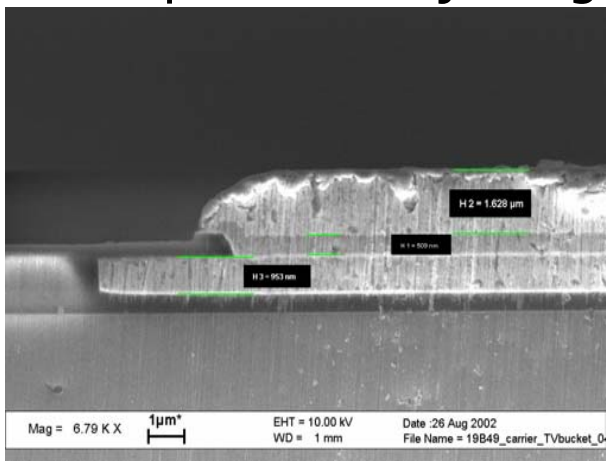


Si Carrier Processing Experience

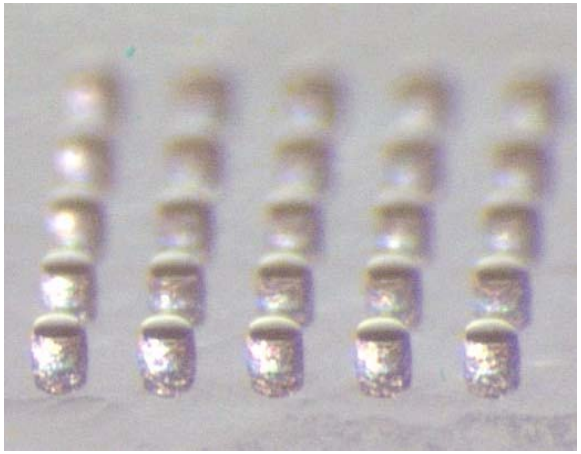
Reactive Ion Etching (RIE) & Sidewall Insulation of vias



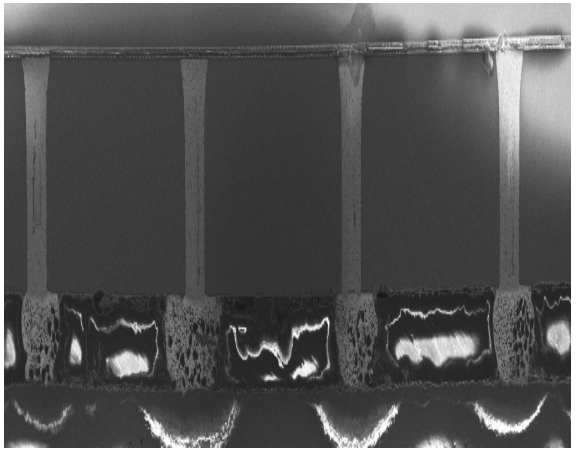
Electroplating of microjoins for chip to carrier joining



Backside wafer grind, polish and exposure of via bottoms

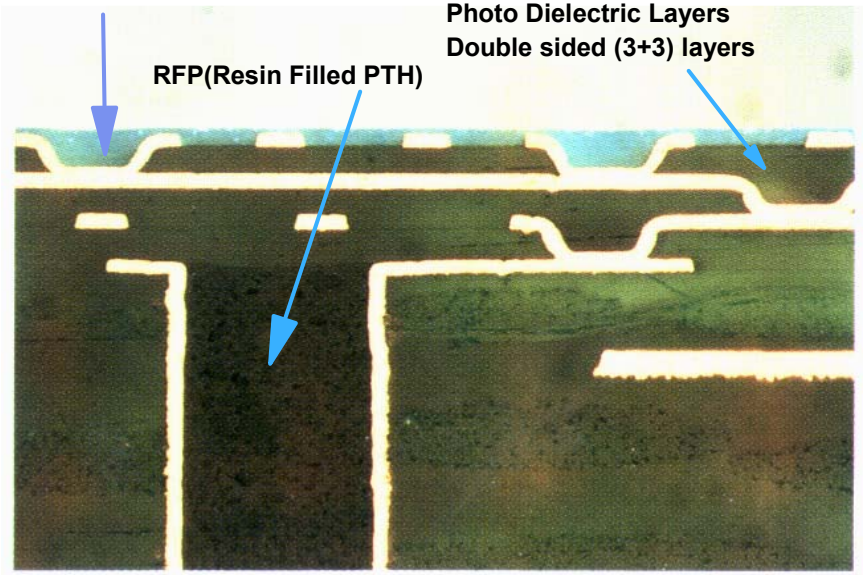


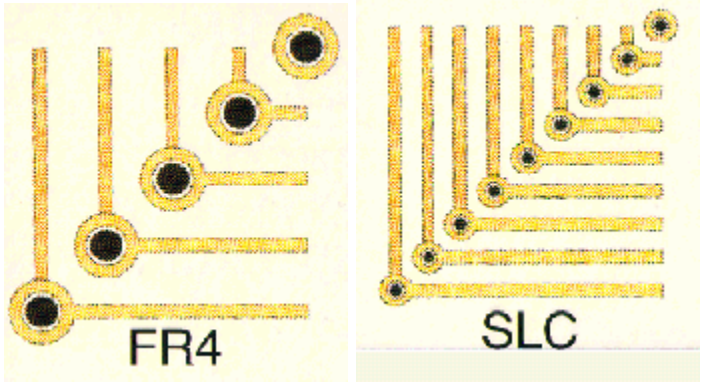
C4 evaporation for carrier assembly on a module/card

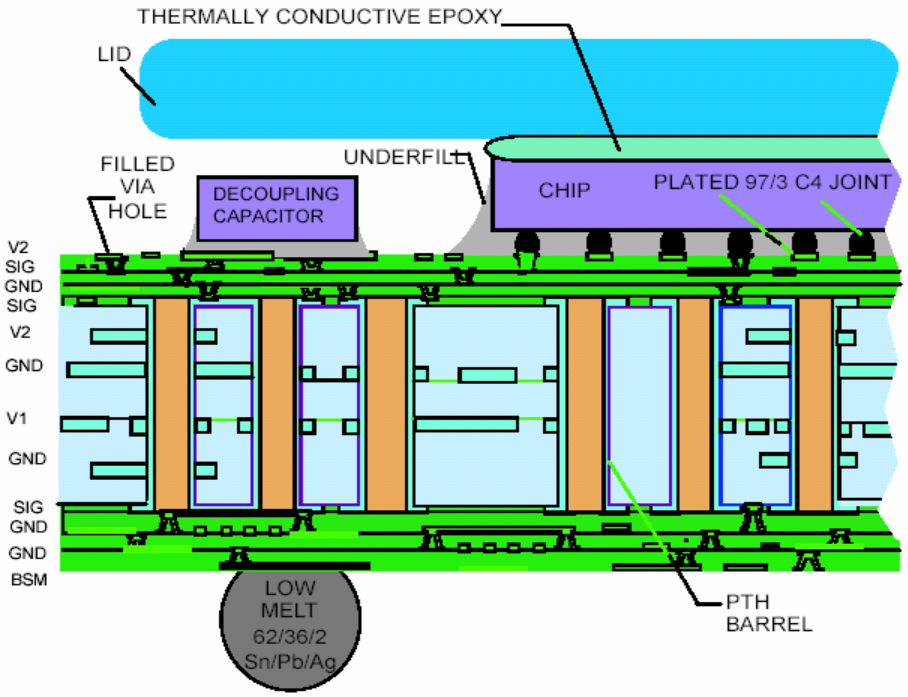


IBM SLC (Surface Laminar Circuit™) Card Technology

Photo Via
Via dia. ; 3.5 mil (90um)/5mil (125um)



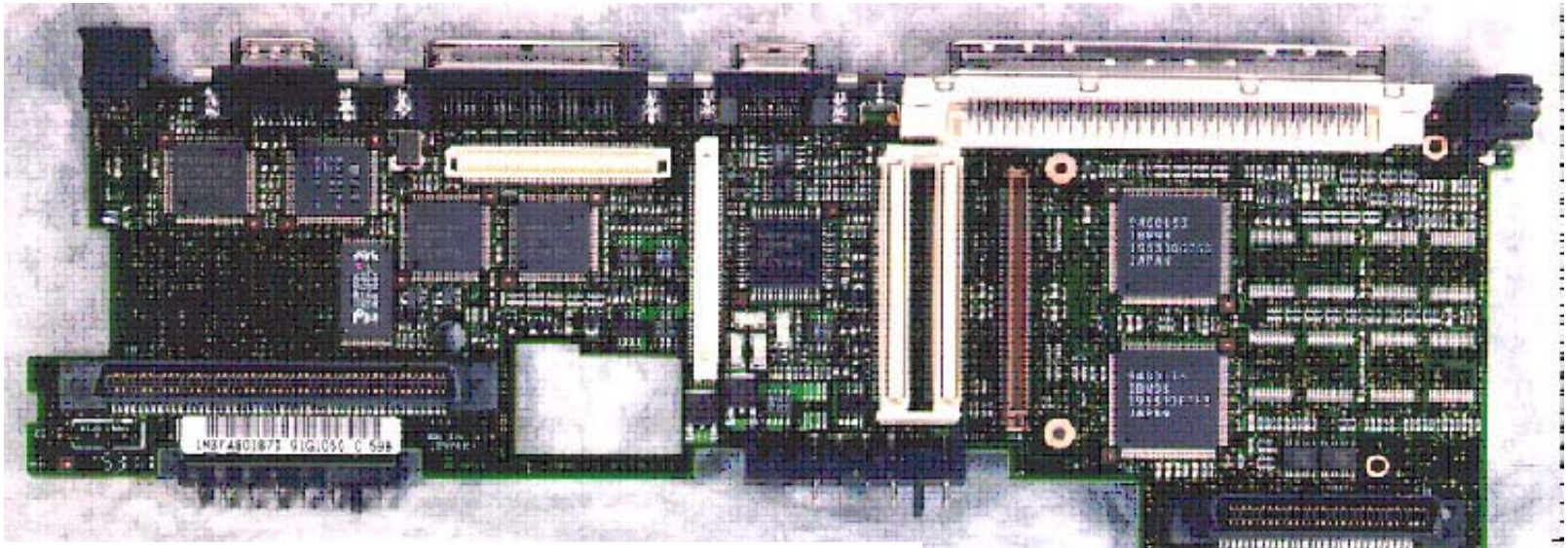




Typical ASIC Cross Section - SLC™ (3-6-3) Module : Flip Chip Plastic Ball Grid Array

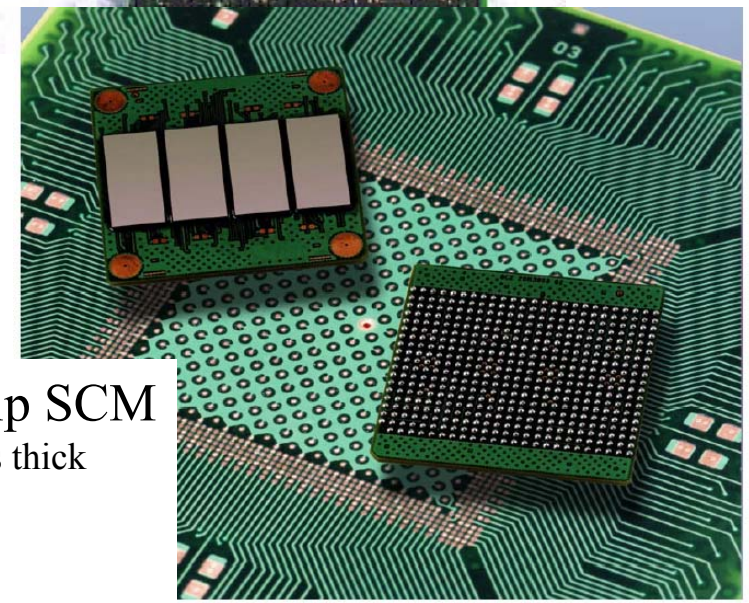
- ✓Increased density
- ✓Improved fan out
- ✓Blind via performance

Present SLC Applications



ThinkPad™ 760CD Base Card

- SLC 6S2P (1+1) 43 mils thick
- 4 mil lines / 4 mil spaces
- 4299 - 5 mil photovias



3-D Graphics Flip Chip SCM

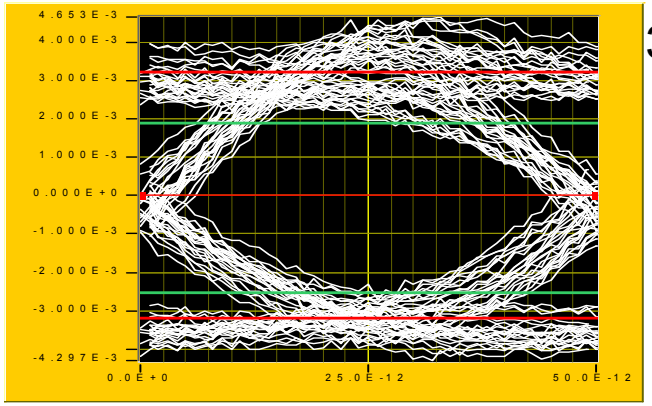
- SLC 2S2P (3+3) RFP 41 mils thick
- 2 mil lines / 3 mil spaces
- 20,880 - 3.5 mil photovias

Optical Bus Design and Test

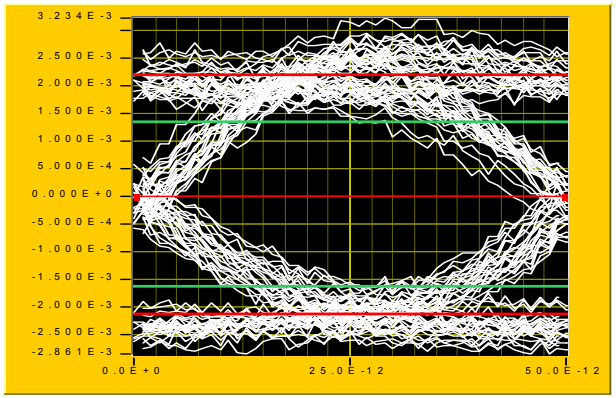
20Gbit/sec, 1KM multimode fiber
VCSEL link
Record bitrate and bitrate*distance

Distance	ISI Penalty	Det. Jitter
2m	1.6dB	11.3ps
300m	1.6dB	10.9ps
700m	2.1dB	13.1ps
1km	2.3dB	13.7ps

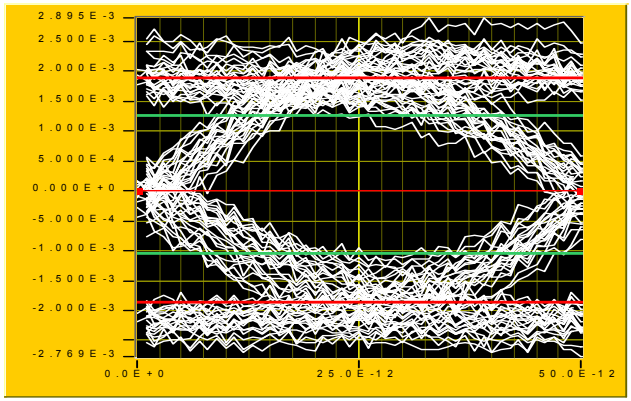
2m



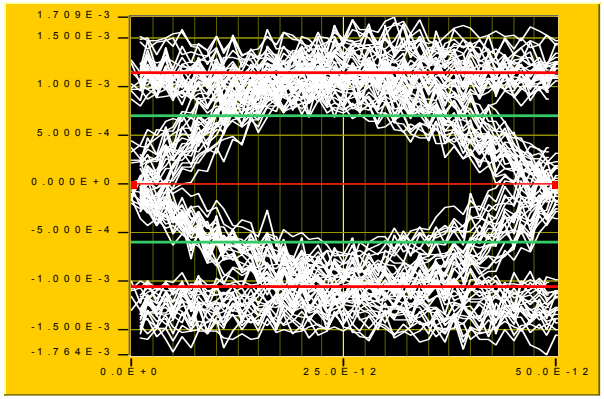
300m



700m

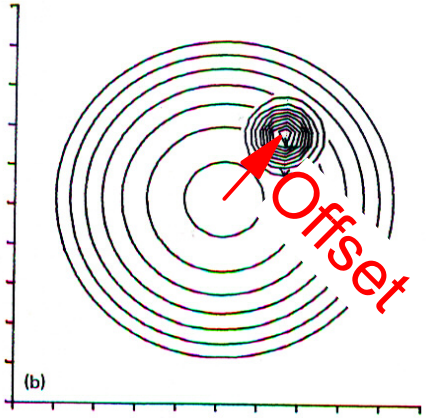


1000m

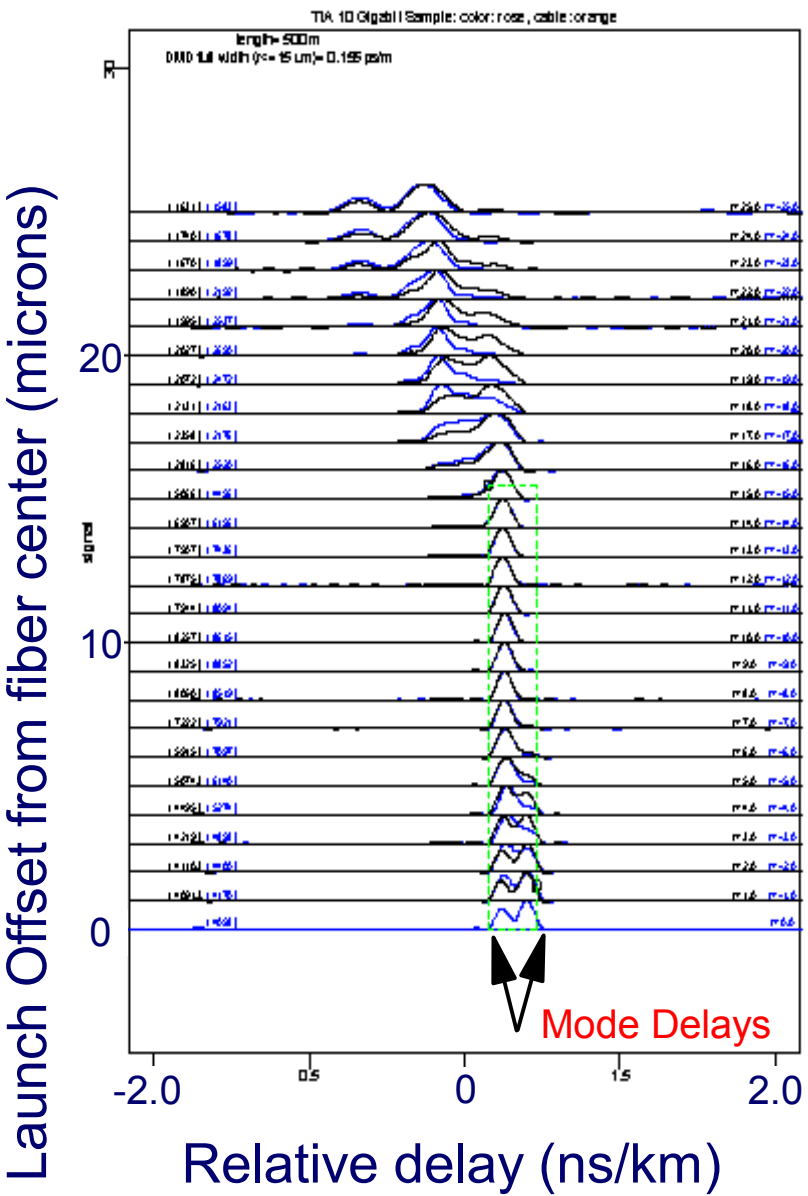


Optical Bus Design and Test

Characterizing the Differential Mode Dispersion of a Multimode Fiber



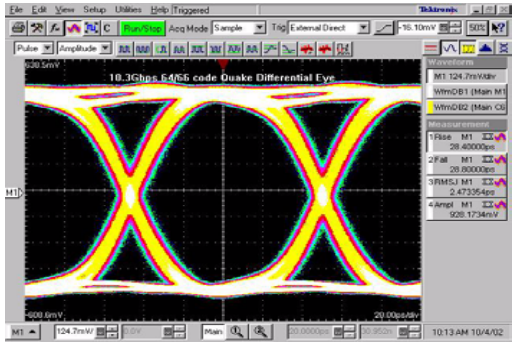
NG MMF NA = 0.21
Restricted Launch NA ~ 0.1



Optical Bus Design and Test

Parallel 120Gbit/sec tester

- 12 Differential Outputs, 9.9-11.0Gb/s/ch
  - Tr, Tf <30ps
  - Low Skew <6ps/channel
  - Adjustable amplitude, 500mV-2.0V differential
- 12 Differential Inputs
  - Error Counter for PRBS31
  - Clock recovery on each channel
- 4 User Selectable Data/Test Patterns
  - PRBS31, Square Wave, AnBn, 64/66
    - First three can be error checked with Commercial tester
- Computer Controlled
  - Individual channels have enable/disable for Xtalk testing
- Very Very Low Cost!!
  - Built from 100% commercially available components
  - ~30x lower than comparable commercial tester ($1.5M)
- Also 48 differential I/O channels for 3Gb/s parallel testing

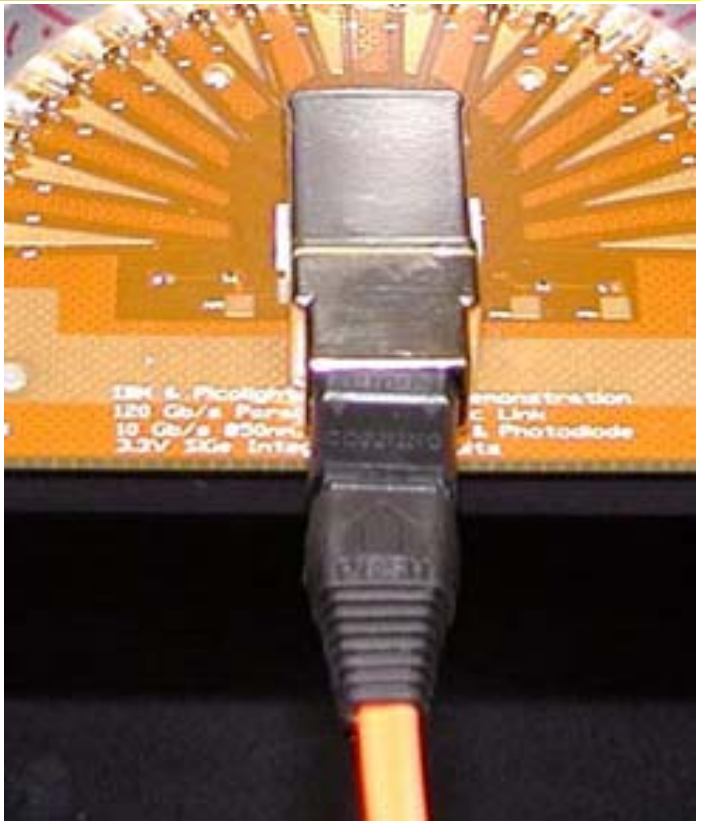


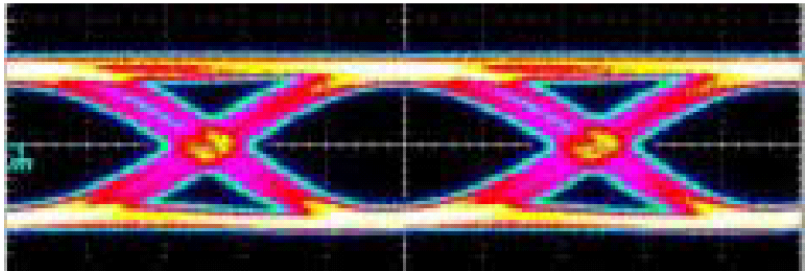
Electrical eye diagram at 10Gbps

Assembly and Demo Experience

12 channel transmitter at 10Gbit/sec/channel

- Commercial parallel modules not presently available at 10Gbit/sec/ serial rate
  - Commercial designs: 12 channels at 2.5Gbit/sec/channel
  - Create and model a prototype parallel optical transmitter with 12 channels at 10Gbit/sec/channel.
- Based on Picolight commercial 3Gbit/sec design
  - Demonstrate extension of present technology to next generation
- Modules based on:
  - IBM Research designed SiGe laser diode driver
  - 10Gbit/sec lasers from commercial module mfr.
  - IBM designed electrical flex packaging based
  - on mfrs. existing design techniques
  - Picolight optical alignment techniques





Eye diagram at 10Gbit/sec