

# Chip-to-Chip Optical Interconnects Kick-off Meeting



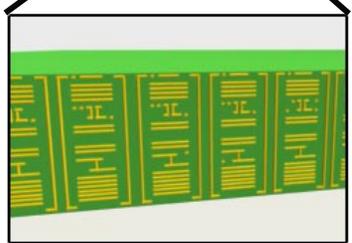
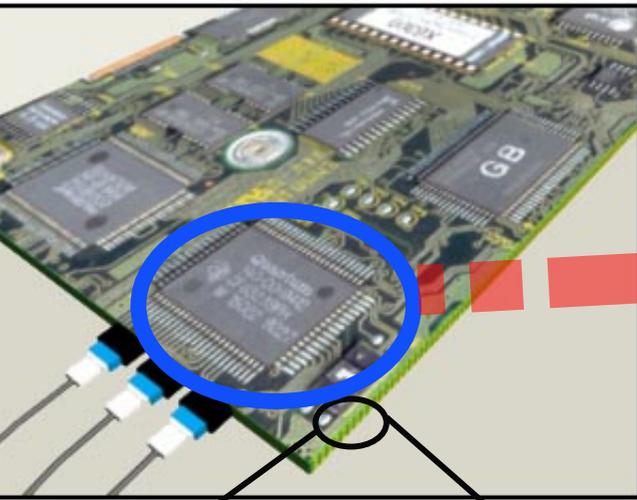
**Ravi Athale, Ph.D.**  
**DARPA/MTO**

**June 23, 2003**

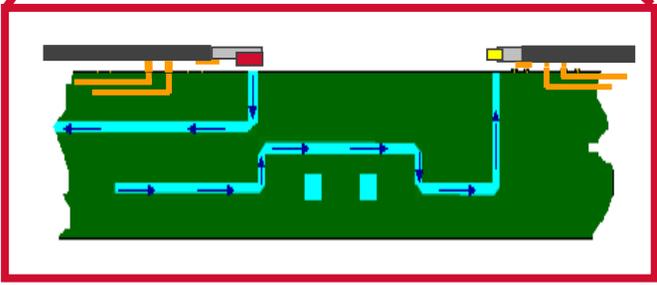
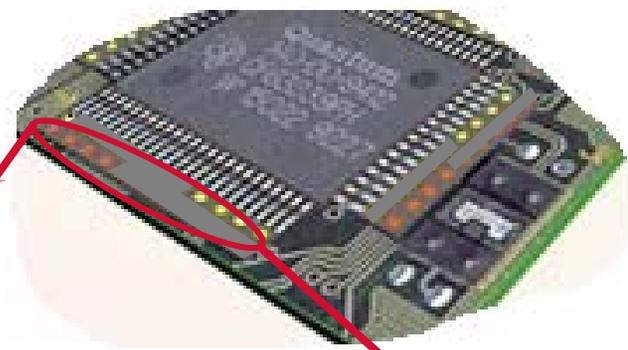


# Chip-Chip Optical Interconnects (C2OI)

## Present Interconnects



## Proposed Chip-Chip Optical Interconnects

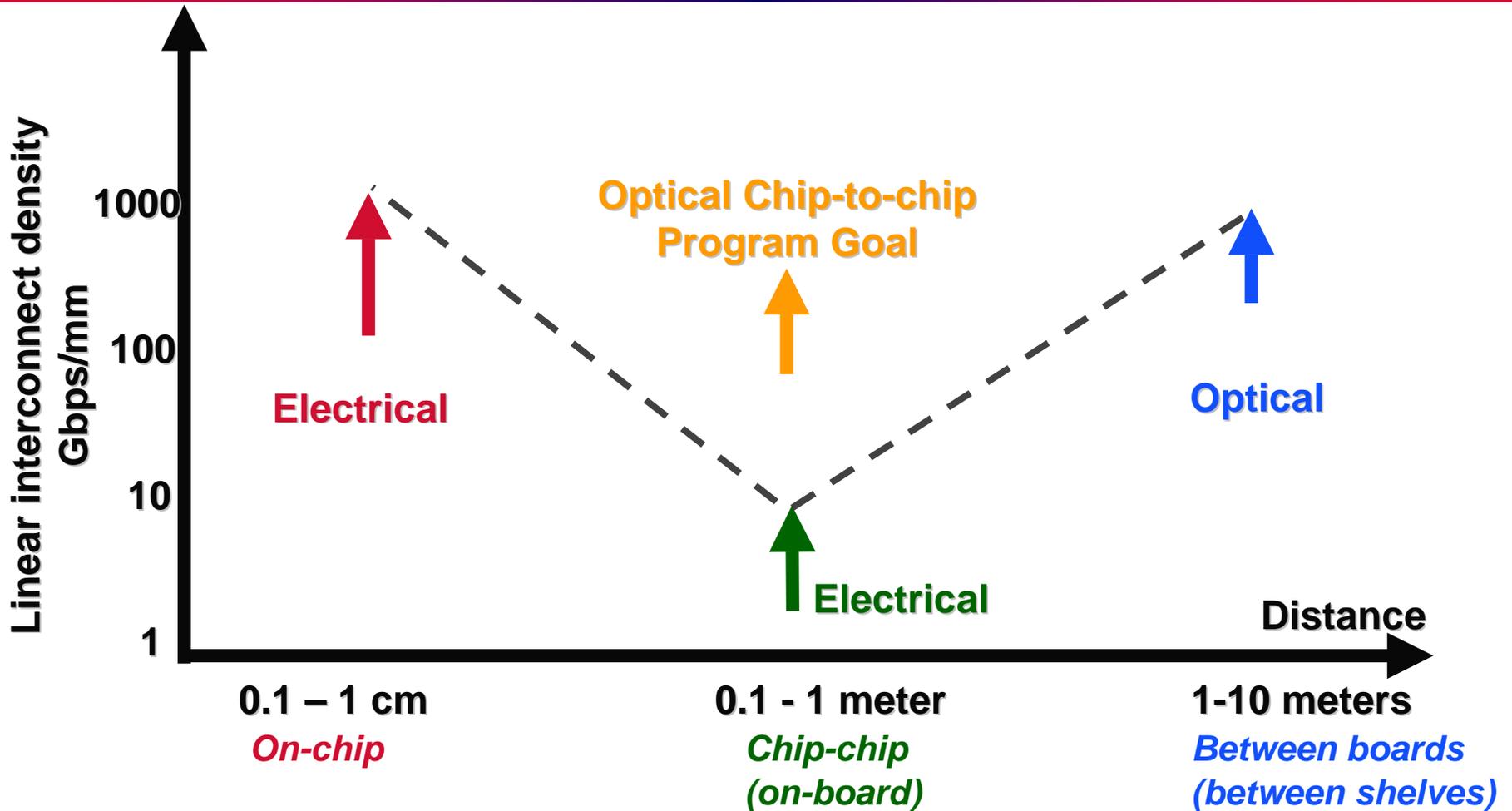


- Objectives:**
- Match off-chip data rate with on-chip data rate
  - Increase total data throughput between chips
  - Enable new sensor signal processing architectures





# Program Goal



## Unique features of optical interconnects:

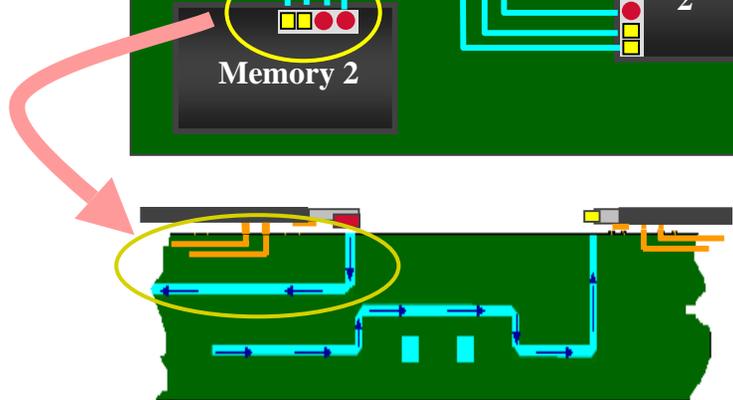
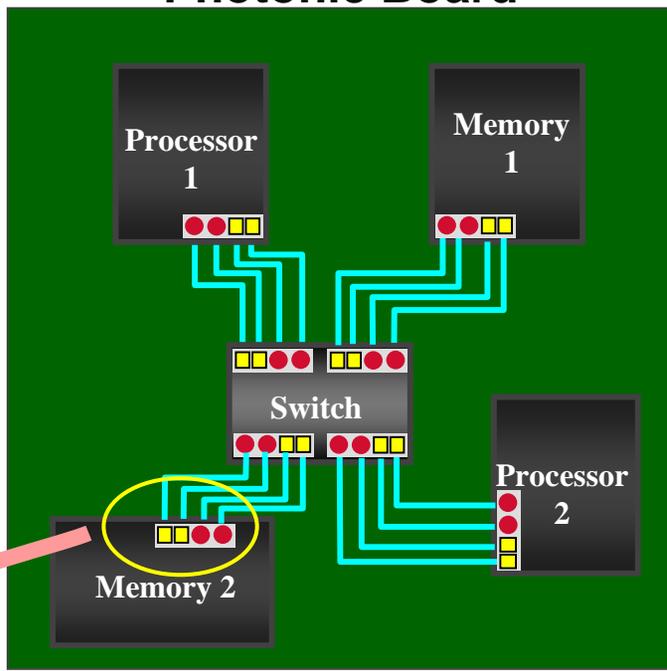
- Scalable bandwidth
- Greater signal integrity
- Lower power





# C2OI Technical Challenges

## Planar (Projected) View of Photonic Board



- ### Optical Channels:
- High linear density (**Density**)
  - Flexible layout (**Layout**)
    - 90 degree turns, Multi-layer
  - Source/detector coupling (**Coupling**)
  - Low loss (**Loss**)
    - Coupling, Propagation
  - Low profile (**Profile**)

- ### Optical Tx/Rx:
- High speed (**Speed**)
  - Low power (**Power**)

- ### Packaging and Integration
- Compatibility with IC packaging (**Chip**)
  - Compatibility with PCB manufacturing (**Board**)

BER

Optical Channel	
Optical Source	
Optical Detector	
Copper Lines	

## Cross-Section View of Photonic Board



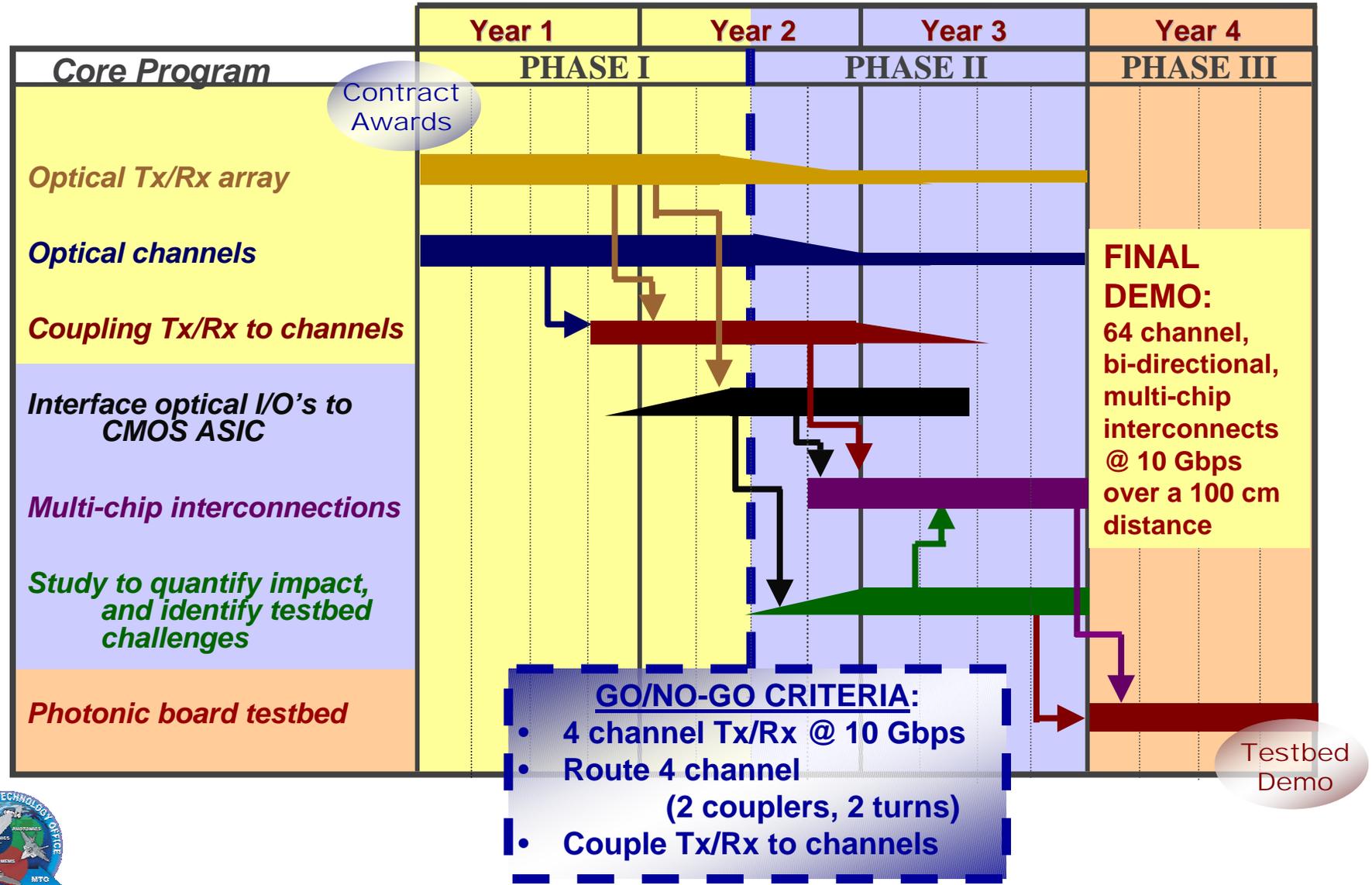


# Technology Attributes

	Today	18 Months	Program Goal
<b>Optical Channels</b>	<b>(OMNET, VLSI-P)</b>		
<b>Density</b>	2 ch/mm (elec) 4 ch/mm (fiber)	8 ch/mm	16 ch/mm
<b>Layout flexibility</b>	12 channel fiber ribbon only	4 channel routing (2 coupling, 2 turns)	64 channel routing (2 layers)
<b>Low profile Length</b>		< 25 mm 30 cm	100 cm
<b>Optical Tx/Rx</b>			
<b>Data rate</b>	3 Gbps/ch (20 Gbps demo)	10 Gbps/ch 4 channels	10 Gbps, 16 ch 40 Gbps, 1 ch
<b>Power dissipation (for 10 Gbps)</b>	200 mW	100 mW	50 mW
<b>BER</b>	1x E-9	1x E-12	1x E-15



# Program Schedule





# Impact of C2OI on Embedded Architecture

- **C2OI** enables equal access integrated architectures.
  - *No chip boundary limitation*
- Integrated architectures offer better computing resource utilization, enabling more efficient algorithms
  - *Non-local memory access-intensive*
- Flattened resource access supports flexible re-allocation of resources optimized for:
  - *Different modes of operation*
  - *Different phases of a mission*
  - *Mission re-planning*





# Interaction with Other DARPA Offices

- IPTO (Bob Graybill)
  - HPCS – Investigating architectural implications of massive interconnects
  - PCA – Adaptive architectures implemented with optical chip-to-chip interconnects
  
- IXO (Bob Hummel)
  - E3D – Processing requirements and data volumes of 3-D sensors and pattern recognition
  
- SPO (Joe Guerci)
  - ISAT – Digital beam forming on space platforms





# C2OI Team Members

- IBM/Agilent:
  - System demonstration
  - 40 Gbps Tx investigation
- UCSB and UT Austin
  - 40 Gbps Tx, amplifier-less 40 Gbps optical Rx
- CSU
  - High speed VCSEL engineering
- Mayo
  - Testing, validation, applications
- ARL
  - Hybrid integration
  - Low power Tx/Rx designs (U Delaware)
- AFRL
  - Polymer material evaluation, waveguide fabrication
- MIT/Lincoln Labs
  - Architecture and insertion studies

