



Independent Study Team SSPS Design



Independent Design Panel

- NIST
- NRL
- Univ. of Wisconsin
- LANL
- NPS
- NSWC Philadelphia
- BMT Syntek Technologies
- Anteon



A Silicon Carbide (SiC) device based Solid State Power Substation (SSPS)

- replace the transformers that exist on the current Aircraft Carrier electrical system
- improve or enable precise voltage regulation, unity power factor, fast fault detection, protection and restoration, easy energy storage, and DC distribution with multiple taps and outputs
- The target application is CVN21.
- 2.7MVA SSPS system converting power as required in the Aircraft Carrier electrical system
 - 13.8kV, 3 ϕ , 60Hz Input
 - 450V, 3 ϕ , 60Hz or 270V_{dc}



SiC SSPS Design Optimized for

- power quality
- recoverability
- weight
- volume
- modularity
- compatibility with CVN21 electric system



SiC SSPS Design Constraints

- Use the following four devices.

Table I: Die level SiC PiN Diodes

Metric	Phase II
T_j (°C)	200
BV (V) ¹	≥ 10,000
V_f (V) ²	≤ 4
I_{on} (A) (DC, discrete die)	≥ 45
Switching frequency (Hz) ³	20,000
Die Yield (%) ⁴	≥ 30

Table II: Die-level SiC MOSFET

Metric	Phase II GNG
T_{jmax} (°C)	200
BV (V) ¹	≥ 10,000
R_{on} (ohm-cm ²)	≤ 0.25
V_{th} (V) ²	5 ± 0.2
$I_{on(max)}$ (A) (discrete die)	≥ 18
Switching frequency (Hz)	20,000
Die Yield (%) ³	≥ 30



SiC SSPS Design Constraints (cont.)

- Use the following four devices. (cont.)

Table III: Die level SiC IGBT

Metric	Phase II GNG
T_{jmax} (°C)	200
BV (V) ¹ (Vce)	≥ 10,000
V_f (V) ²	≤ 6
V_{th} (V) ³	5 ± 0.2
$I_{on(max)}$ (A) (DC, discrete die)	≥ 25
Switching frequency (Hz)	20,000
Die Yield (%) ⁴	≥ 30

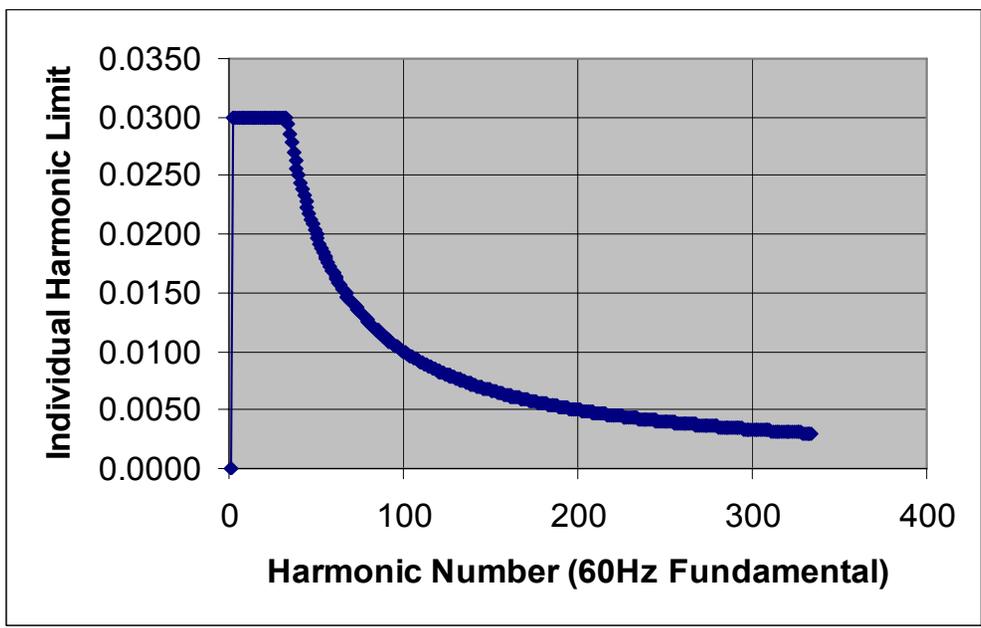
Table IV: Complete SiC Modules

Metric	Phase II GNG
T_{jmax} (°C)	200
BV (V) ¹	≥ 10,000
I_{on} (A) ²	110
Switching Frequency (Hz)	20,000
Configuration	MOSFET/IGBT and PiN diode half bridge module



SiC SSPS Design Assumptions

- Mil-Std 1399 Section 300 A Type 1 quality power on the input and the output of the SSPS.
 - SSPS must subscribe to the load constraints on the MV system.





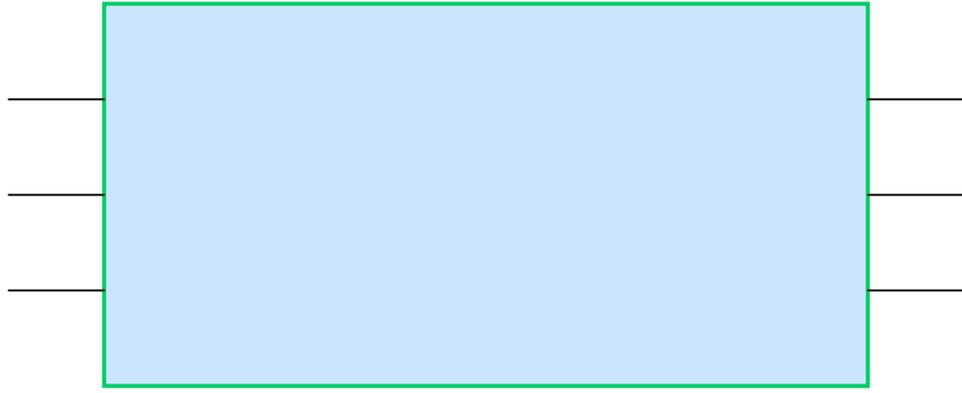
WBG HPE SSPS MOA Requirements

Requirements	
1. Functional Transformer	
2. Improve or enable	
a. voltage regulation	
b. unity power factor	
c. fast fault detection	
d. protection & restoration	
e. energy storage	
f. DC distribution	
3. CVN 21 application	
4. 2.7MVA SSPS accepts 13.8kV 3φ 60Hz input	
a. 450V 3φ 60Hz out	
b. 270V _{dc} out	
Optimize SSPS design for	
power quality	
recoverability	
weight	
volume	
modularity	
compatibility with CVN 21	
Use SiC devices, Tables I-IV	
Derived Requirements	
MilStd 1399 Sec. 300A Type I power	



SSPS Inputs and Outputs

13.8 kVac,
3φ, 60Hz



Type I
(450 Vac,
3φ, 60Hz)

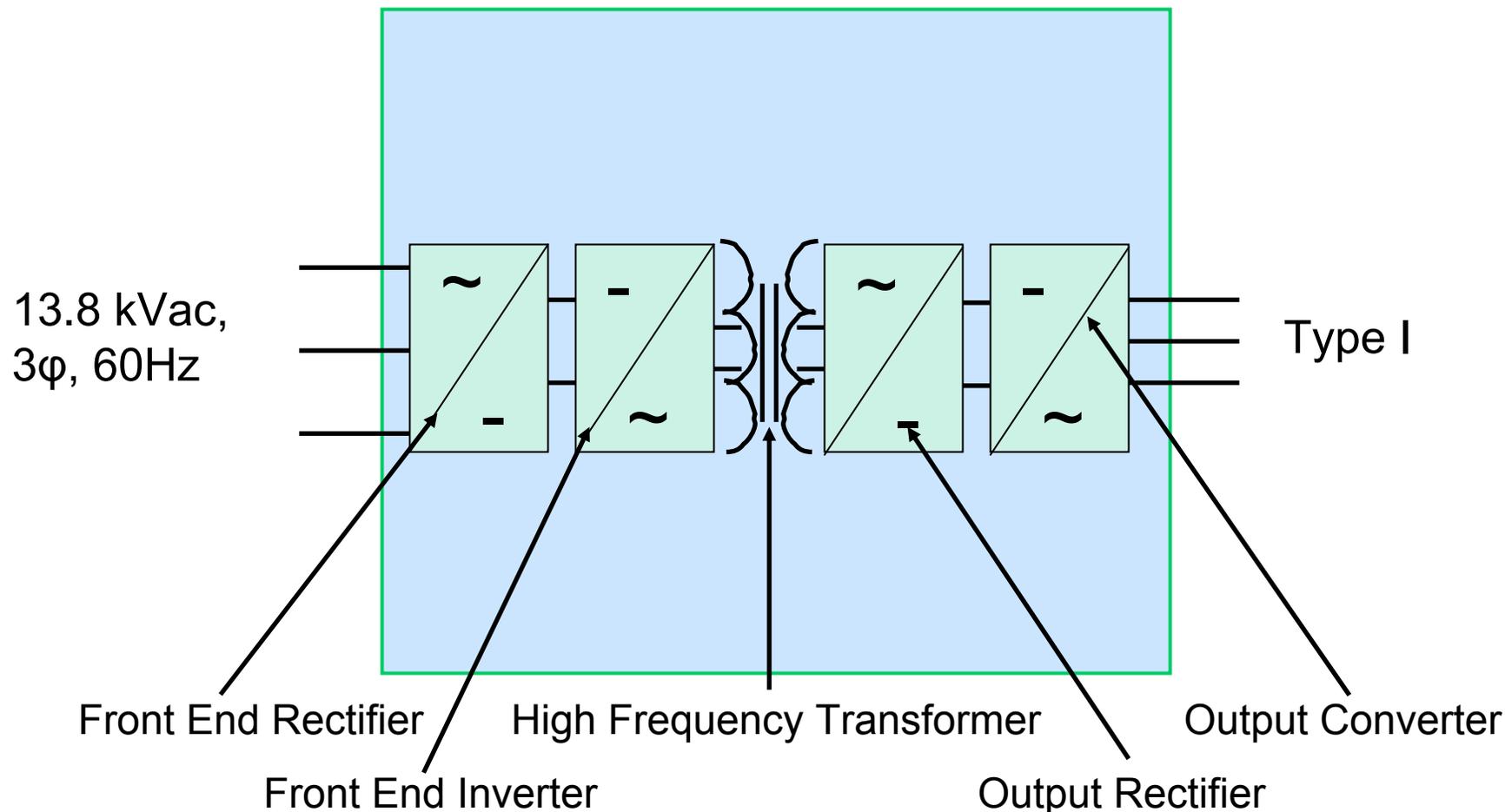
13.8 kVac,
3φ, 60Hz



Type I
Type III
Vdc (270Vdc)



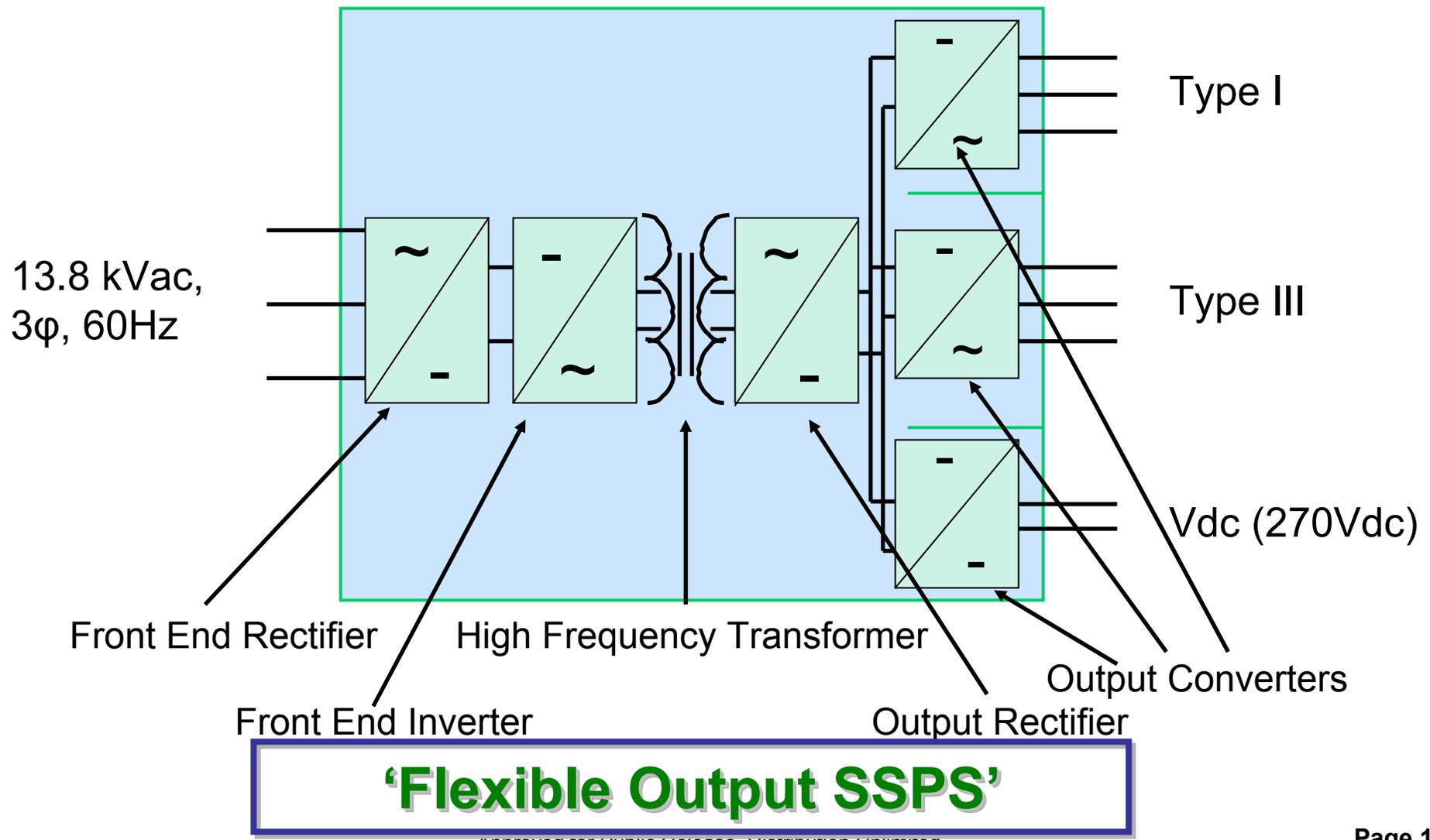
SSPS Generalized Architecture



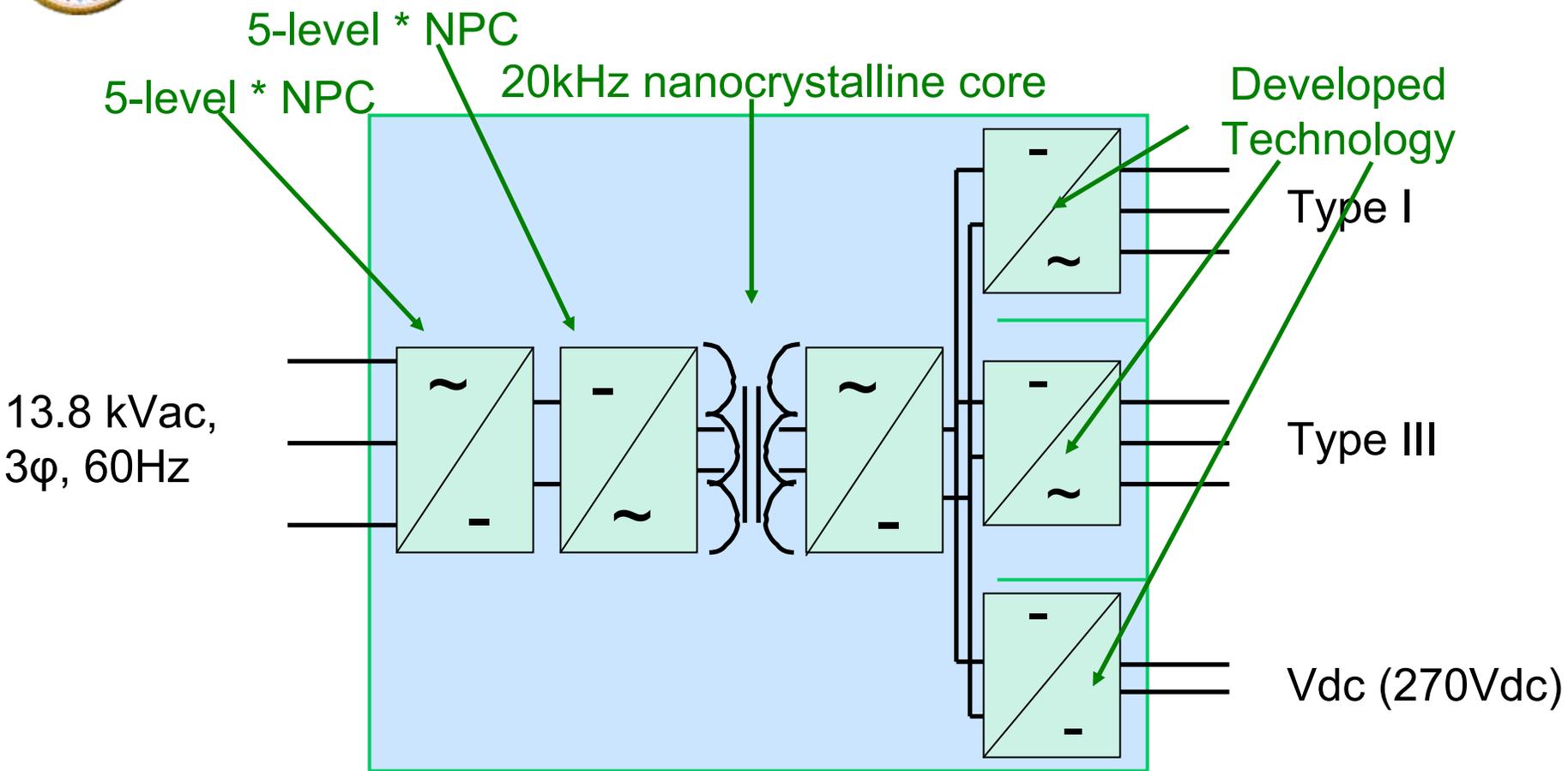
'Integral 3φ SSPS'



SSPS Generalized Architecture



SSPS Design Concept



Concept after Initial Sessions

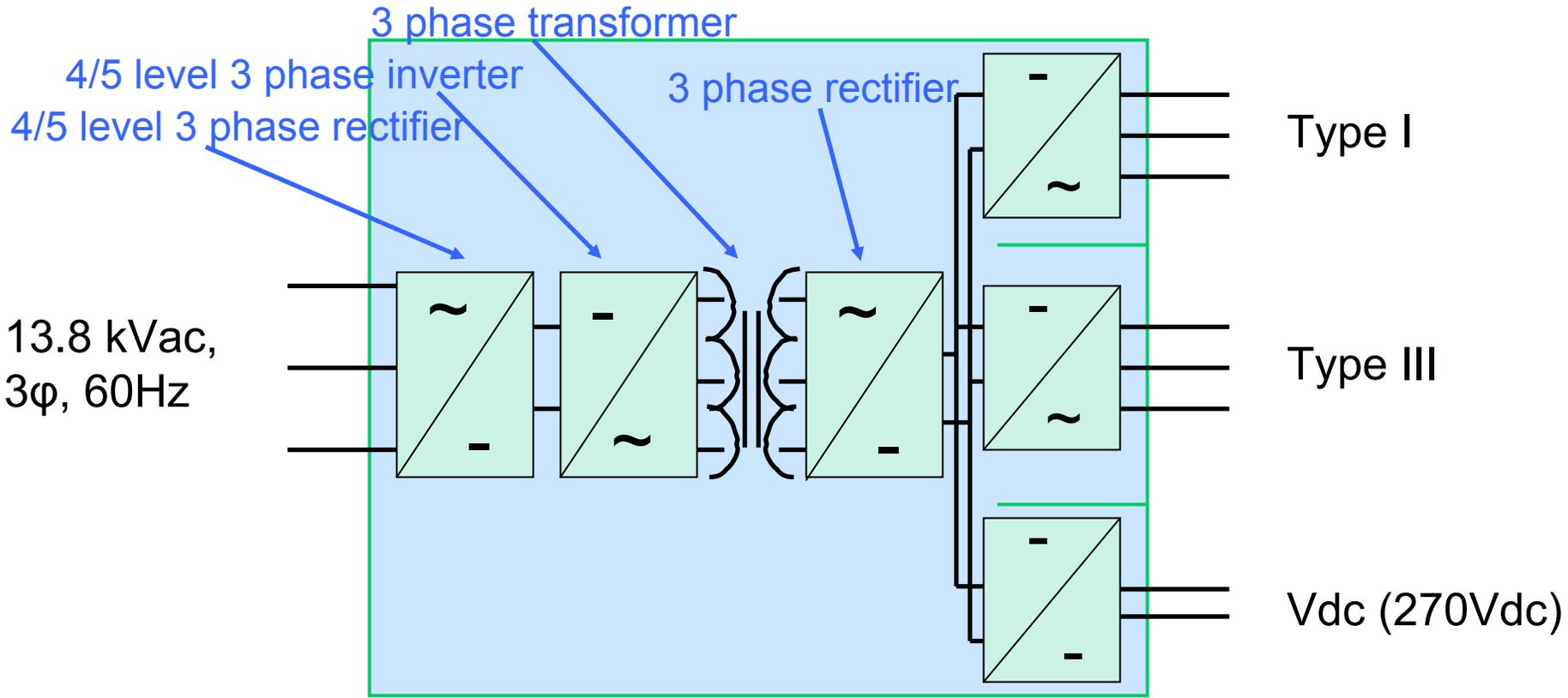


Medium voltage high frequency power distribution system

- Device ratings
 - For a 13.8 kV 3-phase system the peak line to line voltage reaches 19.5 kV, hence to avoid the use of series connected devices a multilevel topology is required.
 - The need for parallel devices cannot be avoided unless the current capability of each device is increased to more than 160 Amps. (2.7 MW @ 13.8 kV)
- 3 level topologies requires 15 kV rating devices
 - Conventional NPC
 - Flying capacitor
 - Force commutated boost rectifier (FCB)
 - Vienna rectifier
 - Cascaded H-bridge
- 4 level topologies requires 10 kV rating devices
 - Conventional NPC
 - Flying capacitor
 - NPC with active mid capacitor voltage control (ACVC)
 - 4 Level + 2 Level rectifier/inverter

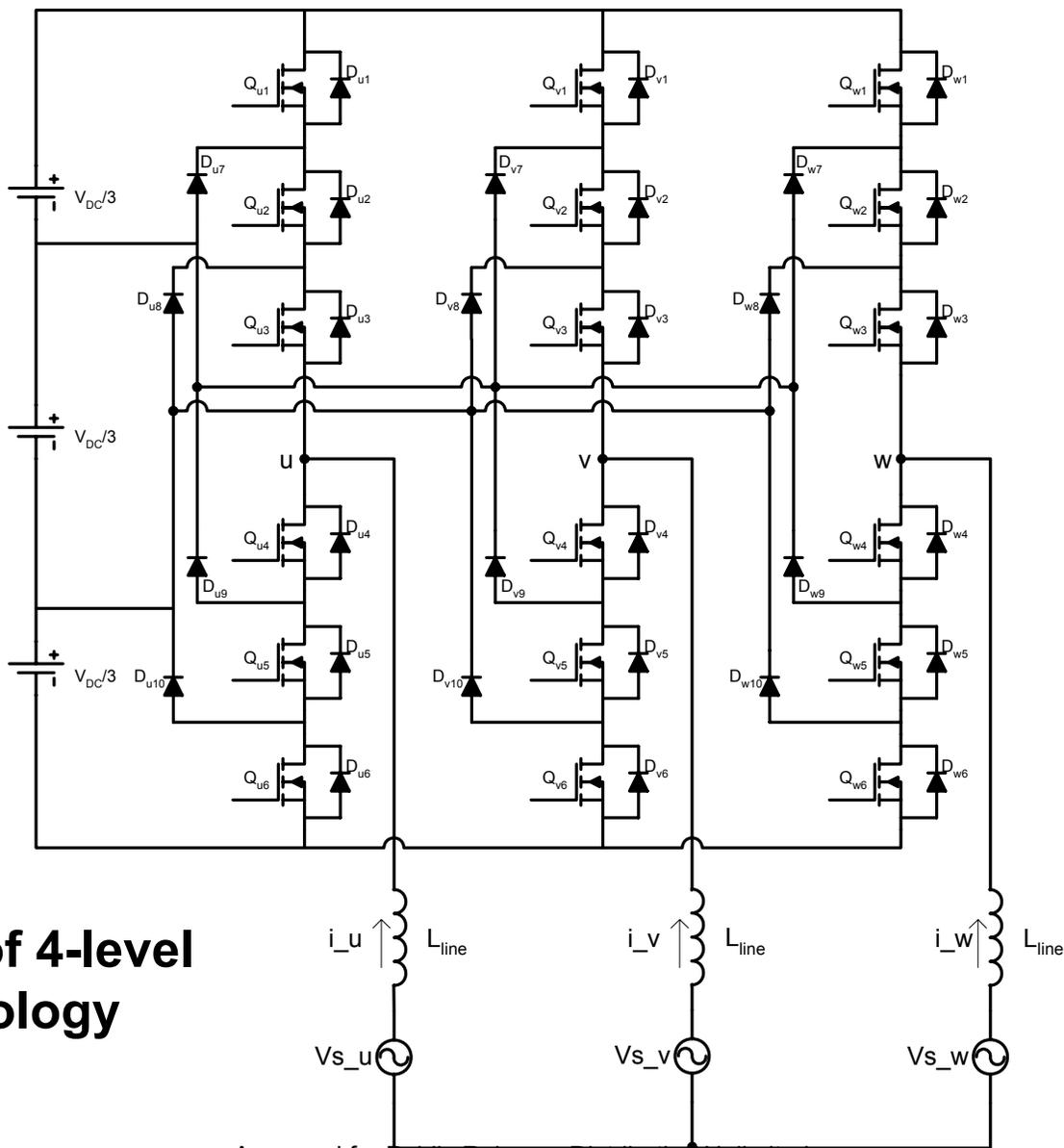


SSPS Design Concept (Revisited)



Notion going into our 13 Sep meeting

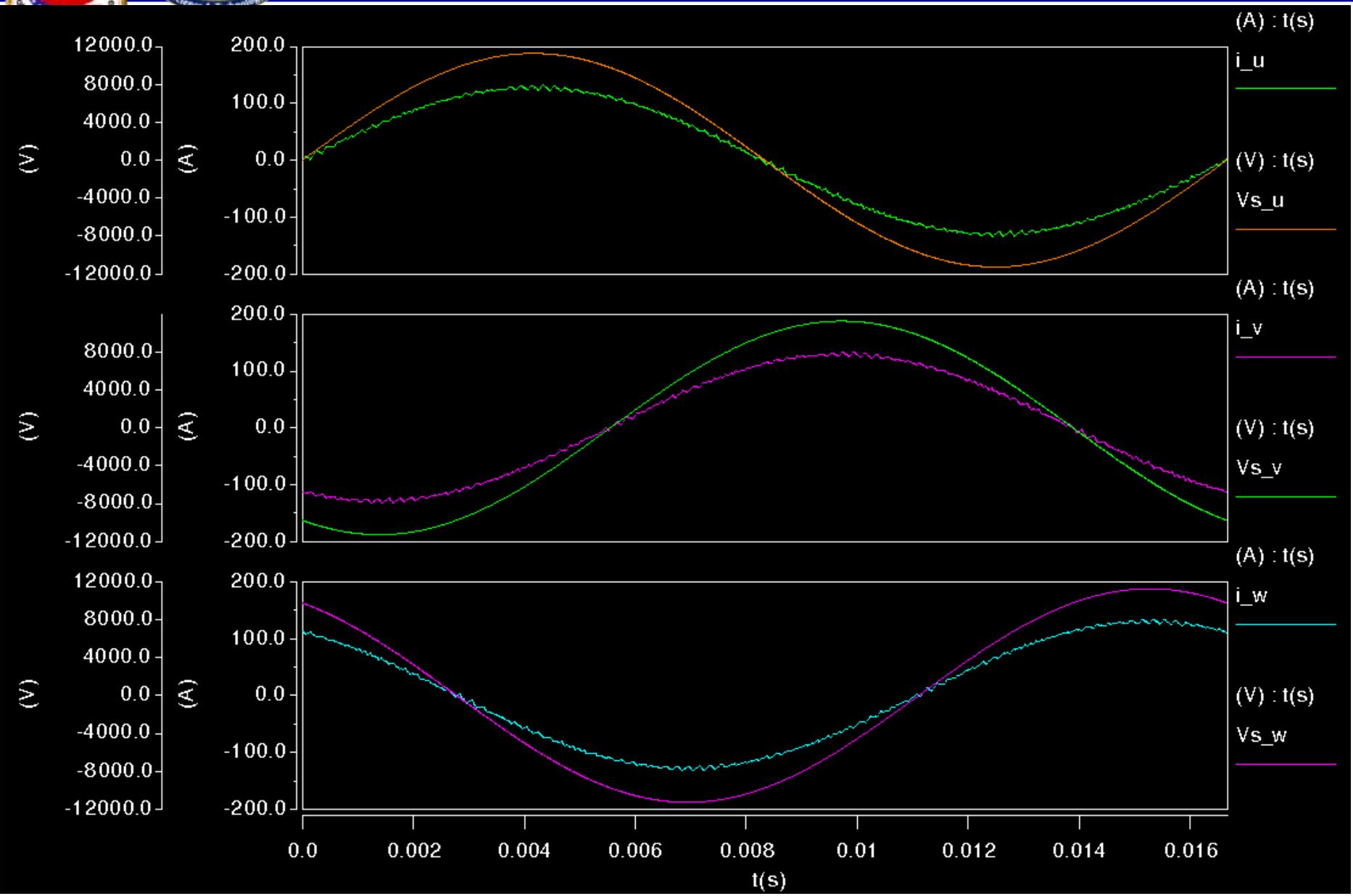
Four-Level Rectifier Topology



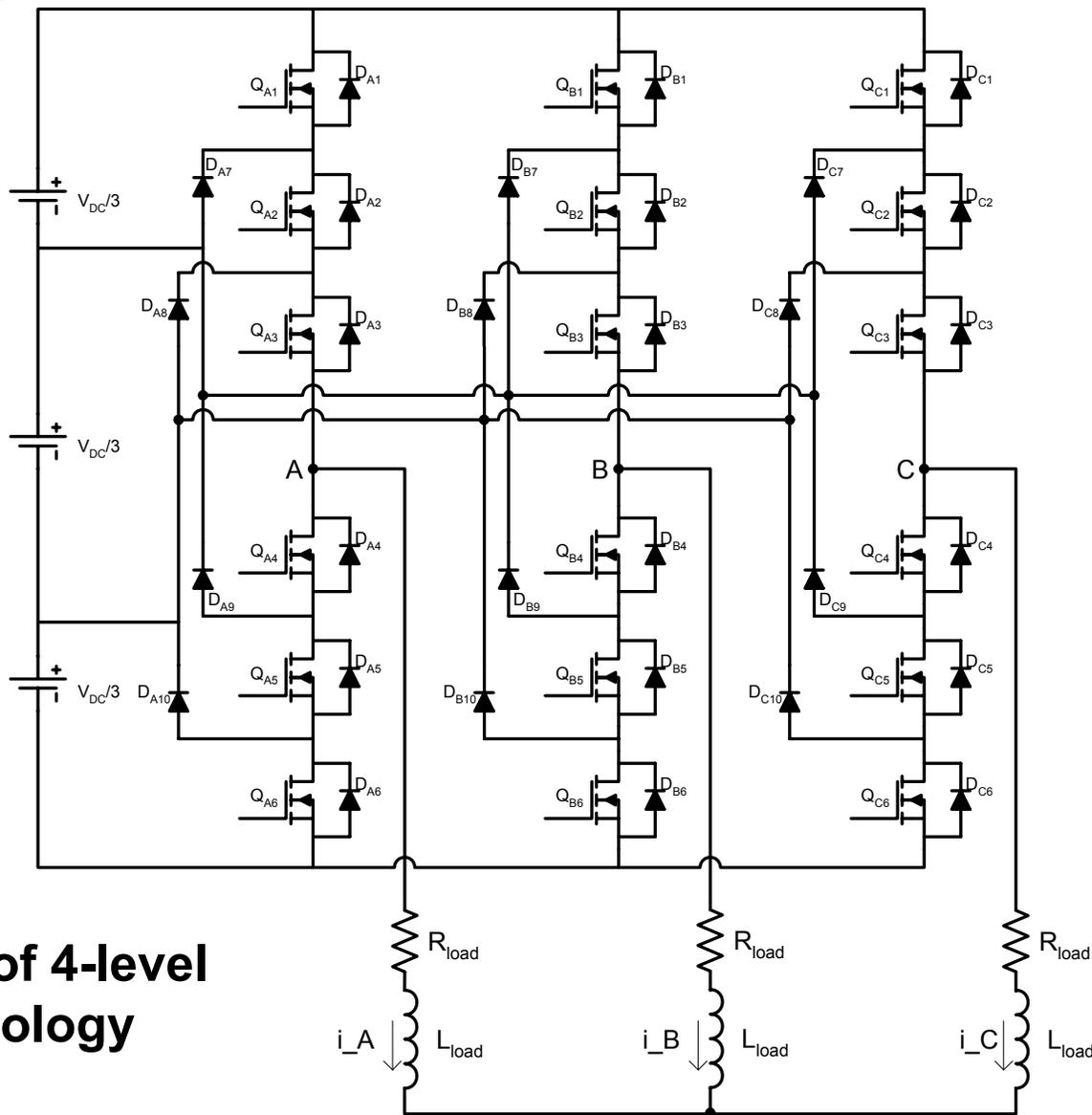
Schematic of 4-level rectifier topology



Input currents and source voltages showing unity power factor



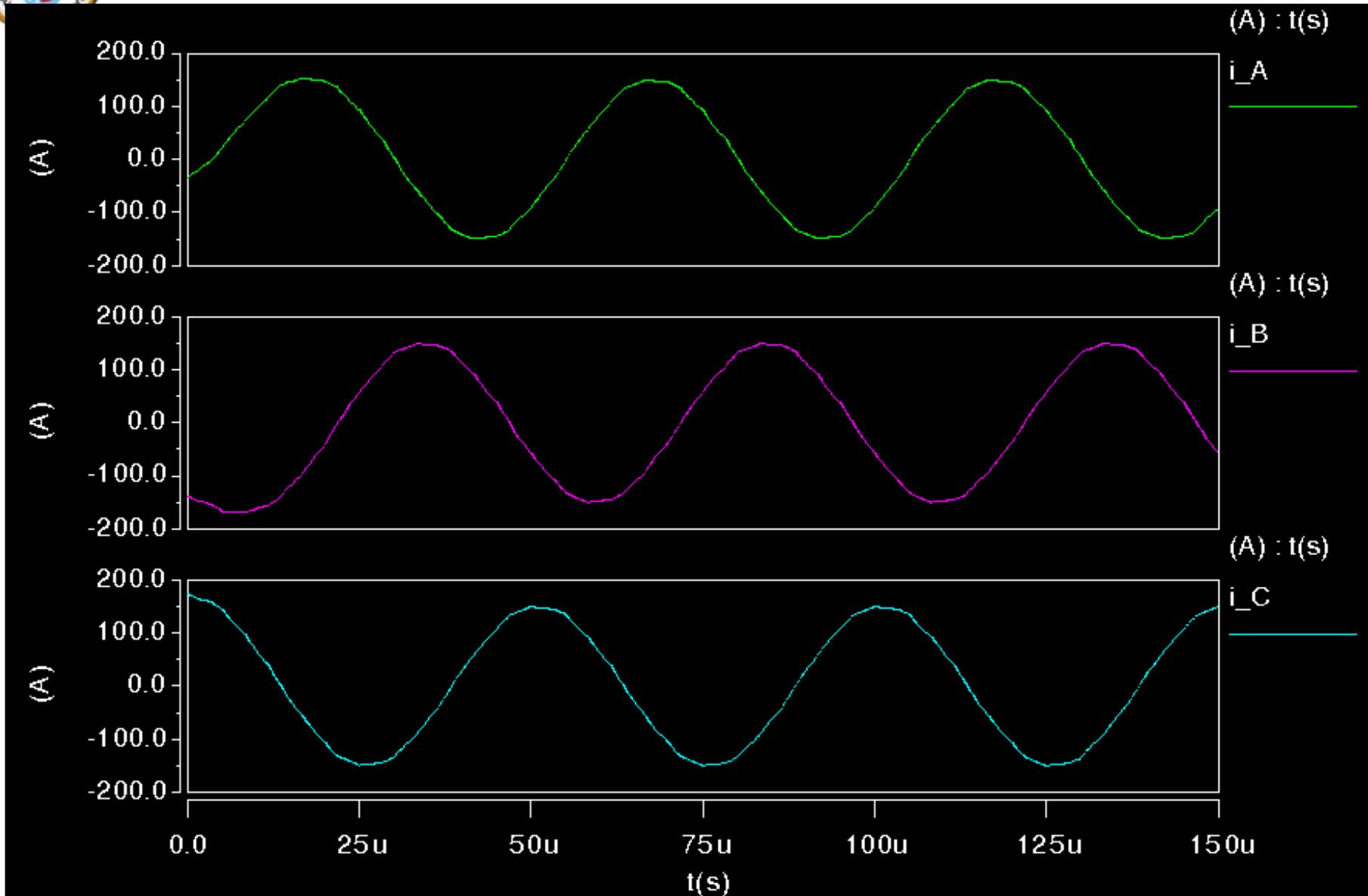
Four-Level Inverter Topology



Schematic of 4-level inverter topology

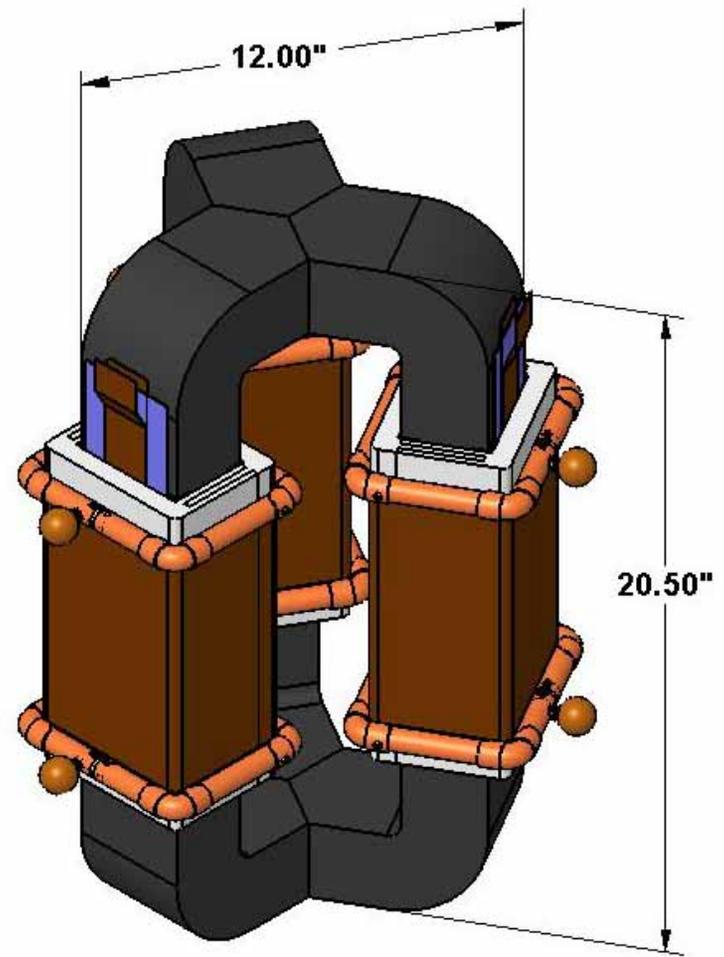


Waveforms of the load current i_A , i_B and i_C (150A peak, 106A rms)

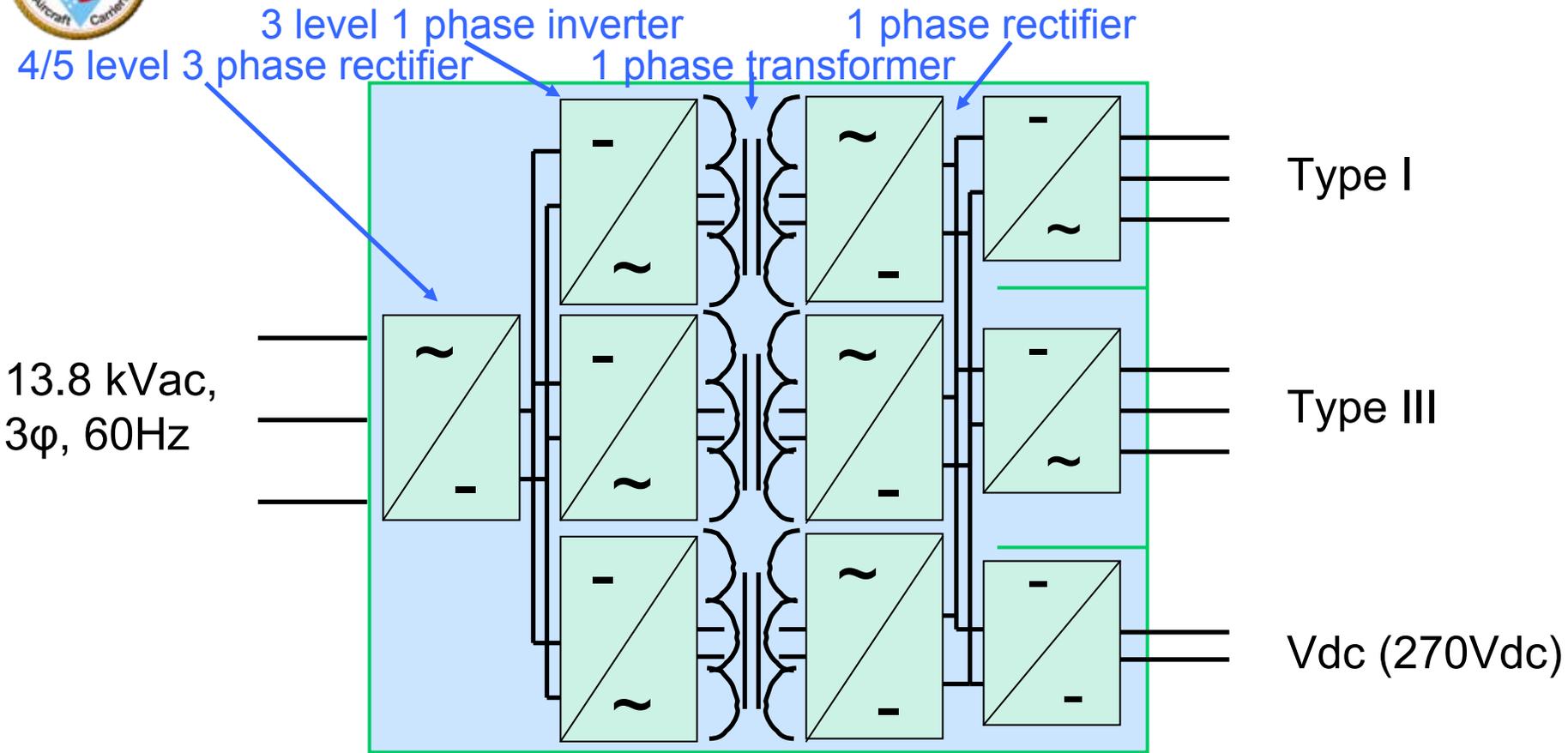




Polyphase Y (2.7 MVA)



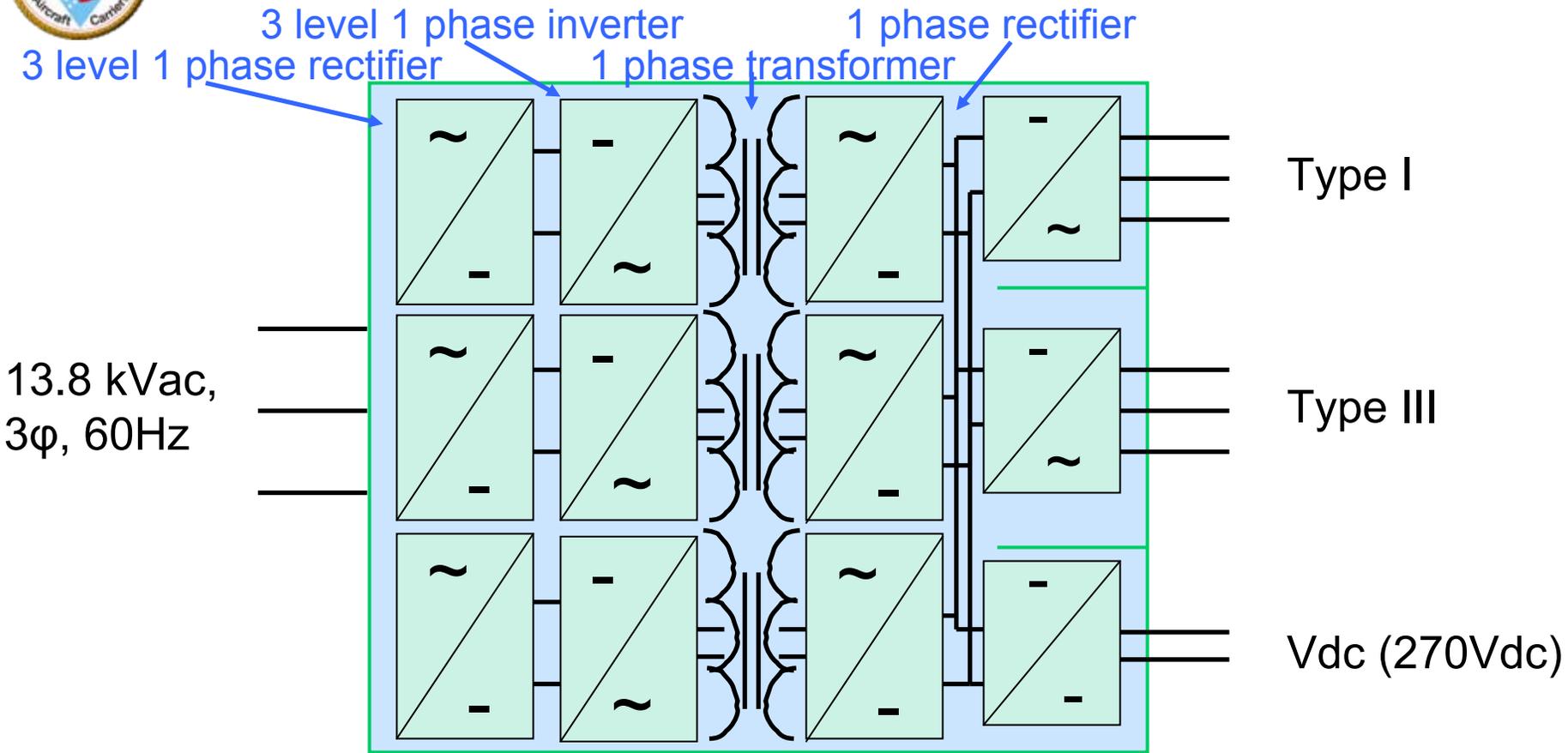
SSPS Design Concept (1 x 3 ϕ)



? 1x3 ϕ or 3x1 ϕ ?

Balanced load to source

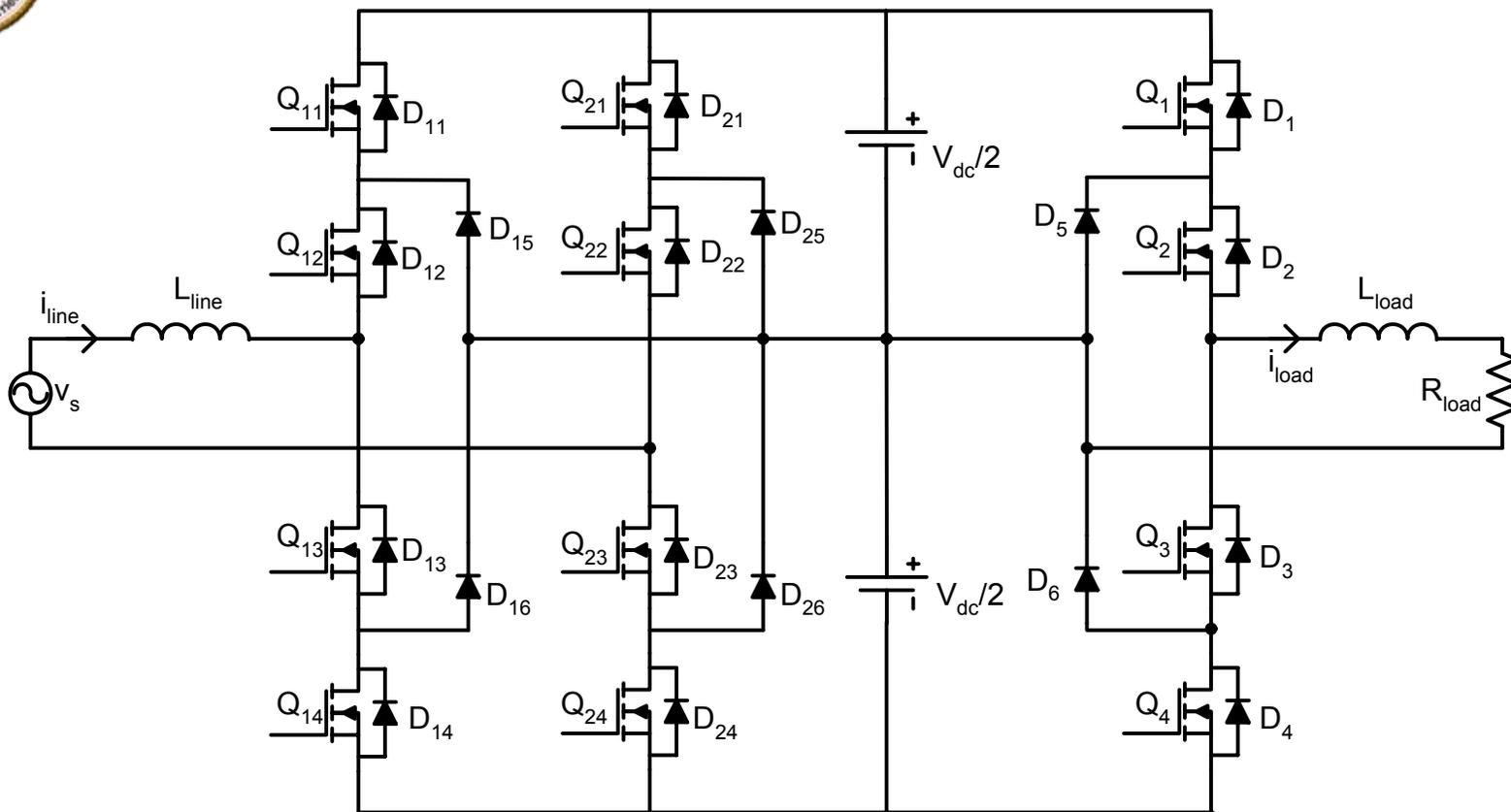
SSPS Design Concept (3 x 1 ϕ)



- It is modular. -

Another good thing – redundancy

Three-Level Rectifier/Inverter Topology

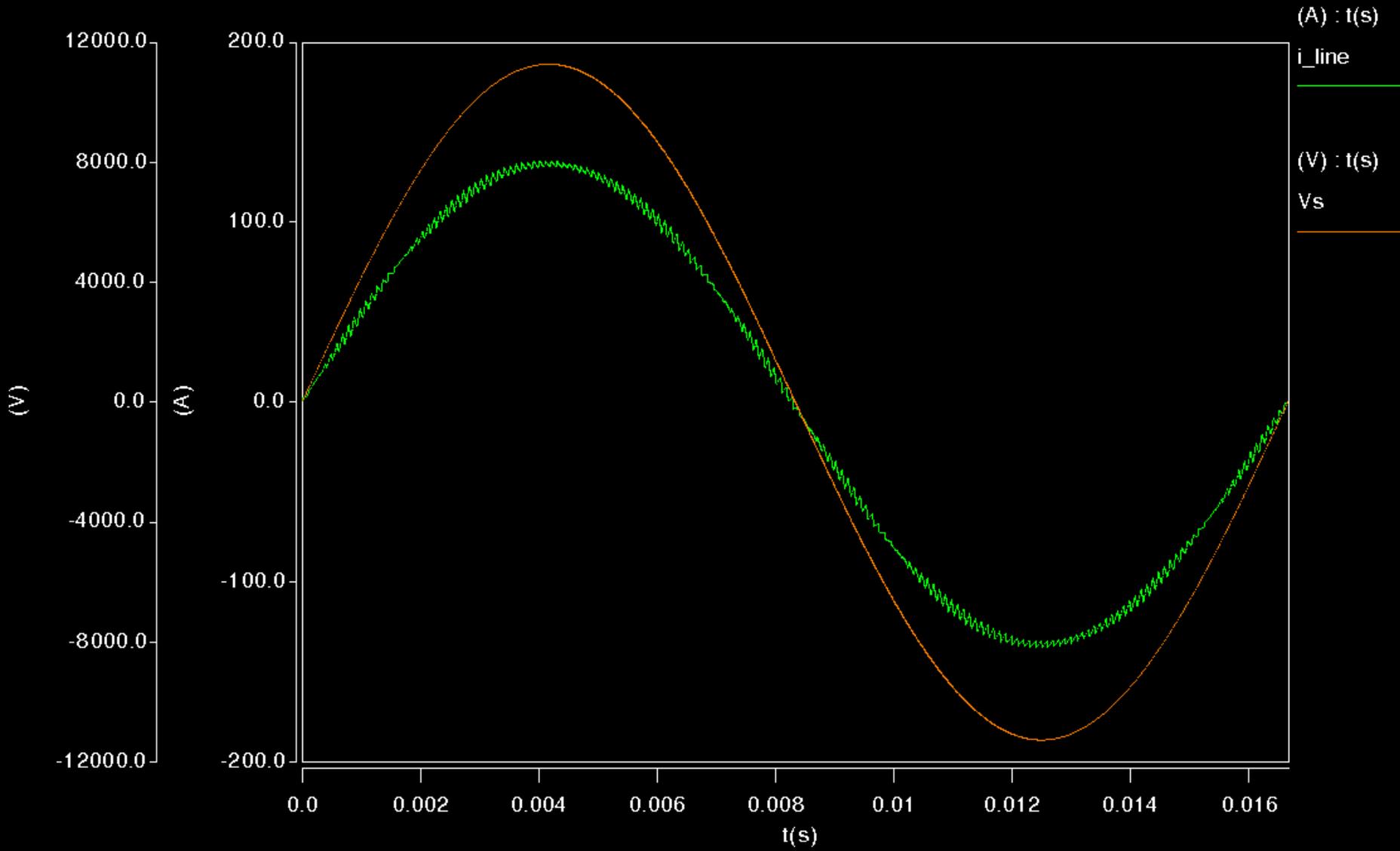


Schematic of three-level single-phase rectifier/inverter topology

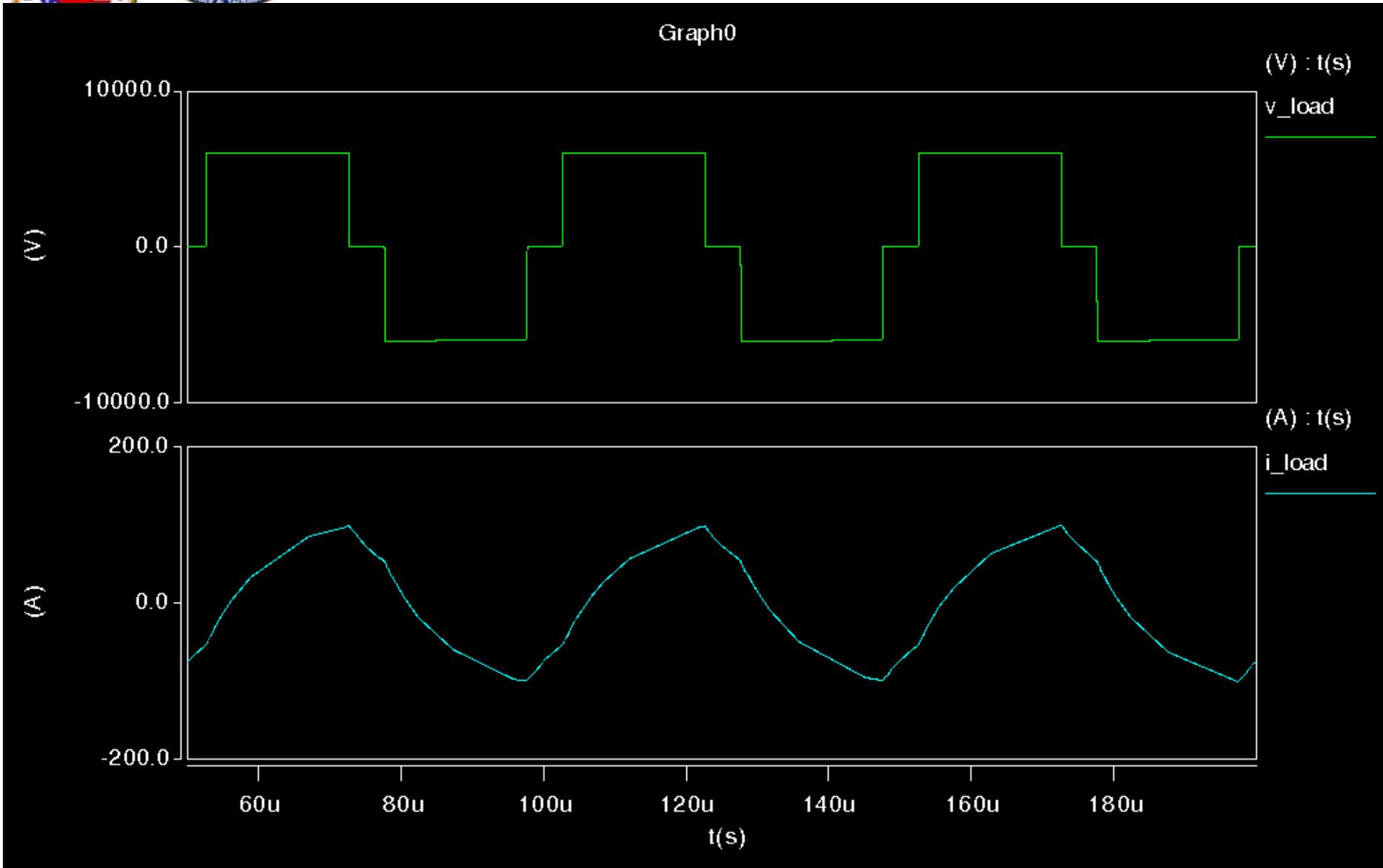


Input current i_{line} and source voltage V_s

Graph0



Load voltage and current

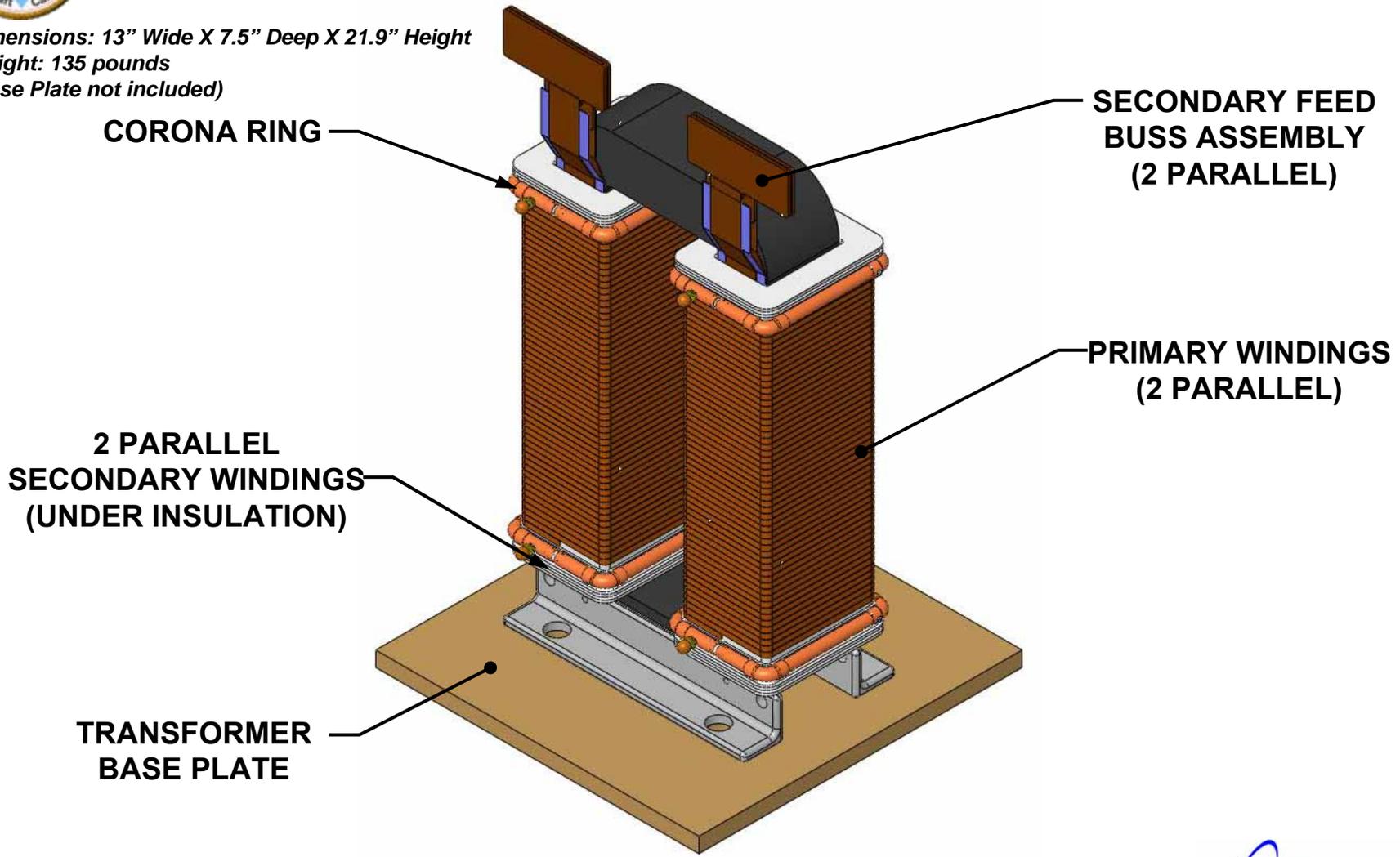


The load cited here is the input to the high frequency transformer.



Core Designs Higher Efficiency & Simplicity

Dimensions: 13" Wide X 7.5" Deep X 21.9" Height
Weight: 135 pounds
(Base Plate not included)





Analysis of Topologies

- MOSFET and diode model validation
- Losses calculation
- Simulated results
 - Three-level line-neutral with Schottky diodes
 - Three-level line-neutral with PiN diodes
 - Four level line-line with Schottky diodes
 - Four level line-line with PiN diodes
- Topology Comparison
- Transformer and output rectifier losses