

# “Introduction To Electronics”



**Dr. Michael Fritze**  
**Young Faculty Award Briefing**  
**Arlington, VA**  
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# DARPA Program Requirements



- **What is the revolutionary new capability enabled by this idea ?**
  - How does this compare to state-of-the-art today ?
- **What are the key risks ?**
- **What is the DoD benefit ?**
- **Why should DoD invest in this ?**
  - Why would commercial investment not suffice ?
- **What are the quantitative performance metrics/targets ?**
  - How will we know we are successful ?



# MTO Electronics Drivers



- **Adapting/Modifying CMOS to meet DoD needs**
  - *Commercial world will only develop technologies with high volume business potential*
  - Si-RF (TEAM)
- **Develop Custom Materials & Technologies for DoD**
  - *Novel materials and devices for high performance RF-Front ends*
  - InP HBT's (TFAST), Sub-mm wave imaging (SWIFT)
  - Highly integrated phased-arrays (SMART), Wide-bandgap sc's (WBGS-RF)
  - Power Electronics (RIPE), Graphene (CERA)
- **Realizing Ultra-Low Power Electronics**
  - Device level (STEEP, ABCS)
  - Design/Architecture (ESE, CLASS)
- **Novel Approaches To Integration**
  - Three dimensional integration (3DIC)
  - Compound Semiconductors on Silicon (COSMOS)
- **Novel Approaches for Heat Dissipation**
  - Thermal Ground Plane (TGP)



# Adapting Commercial CMOS for DoD Mixed Signal Needs

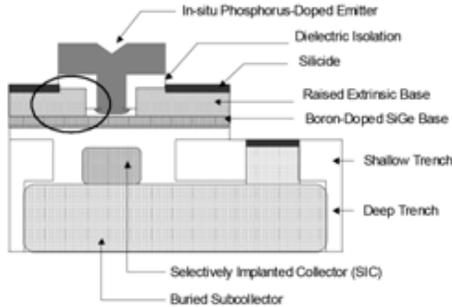


- TEAM Program

- “Technology for Efficient and Agile Mixed-signal microsystems”
- Develop high speed silicon-based mixed signal technology
- No commercial market drivers at these frequencies ( > 300 GHz )



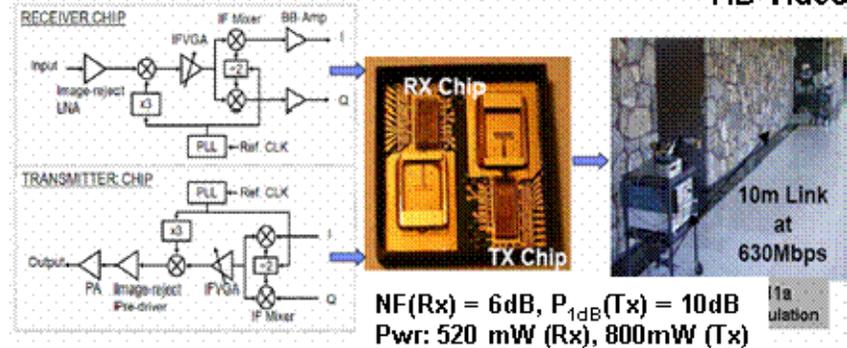
## SiGe RF-BiCMOS Devices



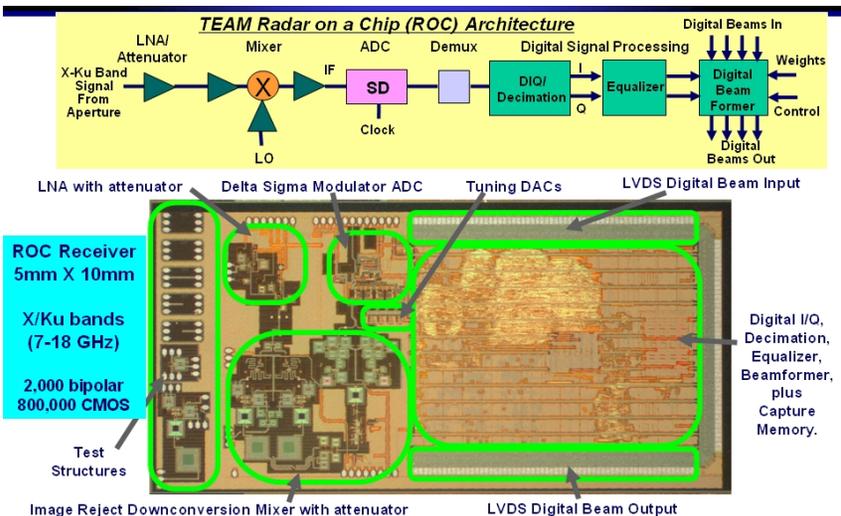
$f_T/f_{max}$  extended to 300/400 GHz

## 60 GHz Transceiver Demo

2 Gb/s  
3.5 m  
HD Video



## SiGe Radar-on-a-chip Receiver



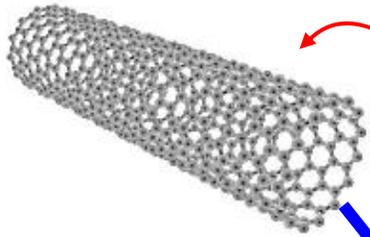
## SiGe EW Receiver



- CERA Program
  - “Carbon Electronics for RF Applications”
  - Develop materials technology for synthesizing high quality graphene over large areas
  - Demonstrate low power RF device/circuit potential of this material



## Carbon Nanotube



Challenges:

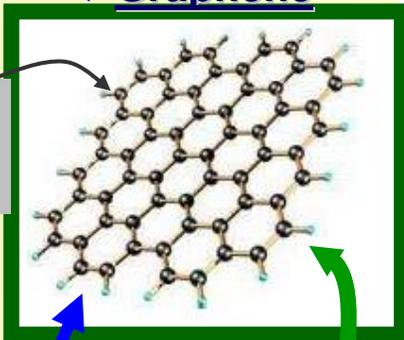
**Placement  
&  
Uniformity**

unroll

## Graphene

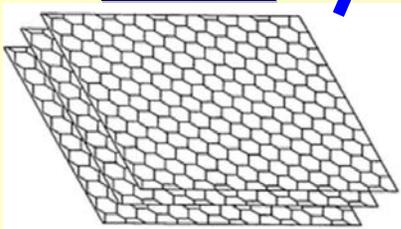
Planar system

$sp^2$  hexagonal  
 $a=0.25\text{nm}$ ,  $c=0.67\text{nm}$   
2D physics



"scrape"

## Graphite



**Planar form has most of  
the desirable properties  
of nanotubes**

## Graphene Properties:

- High mobilities for both electron & hole (10X silicon)
  - $\mu \geq 10,000 \text{ cm}^2/\text{Vs}$
  - mm-wave & low power potential
  - High current density
- Ideal electrostatics ("monolayer-on-insulator")
  - Lattice has sub-nm dimensions
  - Silicon films < 5 nm have mobility decrease
  - Enables aggressive scaling
- Planar processing can be used
  - Standard paradigm
  - Straightforward integration with CMOS
- Semimetal band structure
  - $I_{on}/I_{off} \sim 30$ , useful for RF devices



# CERA: BAA Metrics

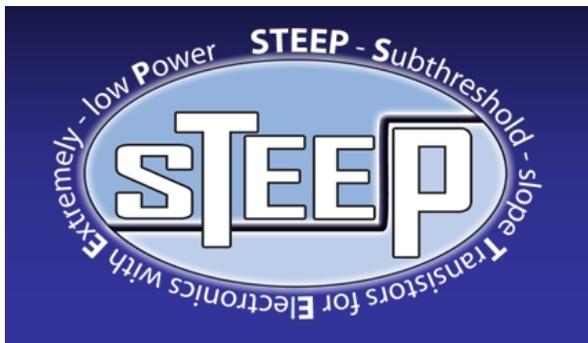


Metric	Unit	Phase I	Phase II	Phase III
<b>GNG Metrics</b>				
Graphene Active Area	mm <sup>2</sup>	50 x 50	Wafer diam. ≥ 100 mm	Wafer diam. ≥ 200 mm
Uniformity	N	N ± 1 <sup>(1)</sup>	N ± 0 <sup>(1)</sup>	N ± 0 <sup>(1)</sup>
Carrier Hall Mobility	cm <sup>2</sup> /Vs	≥ 10,000	≥ 15,000	≥ 15,000
Carrier FET Mobility	cm <sup>2</sup> /Vs	≥ 5,000	≥ 10,000	≥ 15,000
V <sub>ds</sub> (device bias)	V	1.0	0.5	0.25
I <sub>ON</sub> <sup>(2)</sup>	μA/μm	≥ 250	≥ 1000	≥ 2000
I <sub>ON</sub> /I <sub>OFF</sub> <sup>(2)</sup>		10	100	1000
f <sub>t</sub> <sup>(2), (3)</sup>	GHz		> 300	≥ 500
f <sub>max</sub> <sup>(2), (3)</sup>	GHz		> 300	≥ 500
Demonstration Circuit				<b>W-band LNA</b> Frequency ≥ 90 GHz Gain ≥ 15 dB Noise Figure ≤ 1 dB Cross wafer yield ≥ 90%

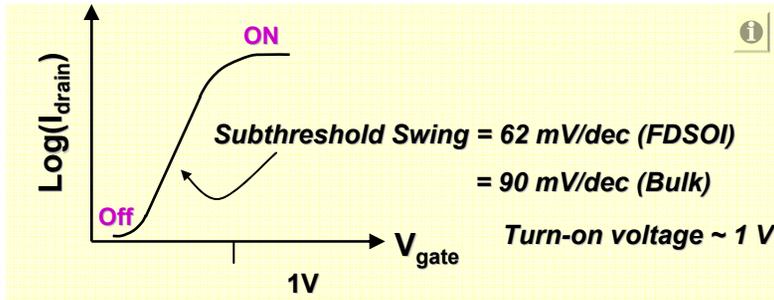
(1) Control number of electrically active layers over required area,  $N \geq 1$

- STEEP Program

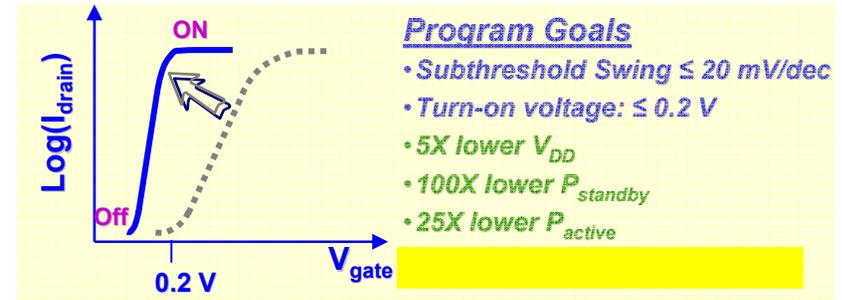
- “Steep-subthreshold-slope Transistors for Electronics with Extrremely-low Power”
- Develop CMOS devices with subthreshold slope  $< 60$  mV/dec
- Demonstrate these devices in ultra-low power circuits



## Today



## STEEP Vision

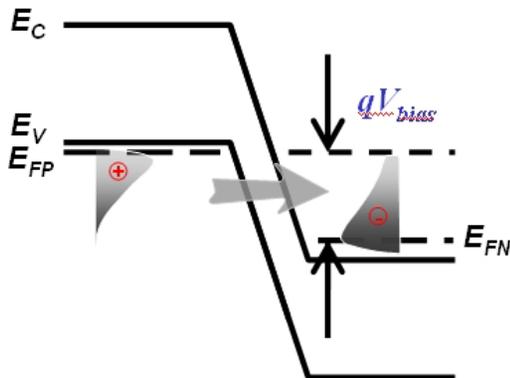


**Theoretical minimum of the subthreshold swing of MOSFET is  $\ln 10(kT/q)$  or 60 mV/dec**

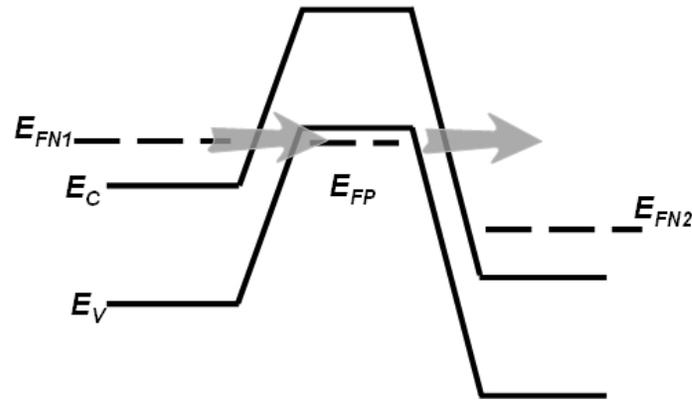
**Develop ideal transistor switch for ultra-low power electronics**

**Band-to-band tunneling device: Sharp band edge “cuts off” high energy electron tail**

(A) Esaki Tunneling Diode



(B) Band-to-band Tunneling Transistor





# STEEP Program Metrics



Metric	Unit	SOA	Phase I	Phase II	Phase III
<b>GNG Metrics</b>					
Subthreshold Swing <sup>(1)</sup>	mV/dec	62	≤ 30	≤ 20	
I <sub>ON</sub> <sup>(1)</sup>	μA/μm	>1000	≥ 200	≥ 1000	
I <sub>OFF</sub> <sup>(1)</sup>	nA/μm	>100	≤ 100	≤ 10	
V <sub>dd</sub> <sup>(1)</sup>	V	~1	≤ 0.5	≤ 0.2	
Delay (CV/I)	psec	< 5	NA	< 5	
Device Uniformity (I <sub>ON</sub> , V <sub>T</sub> ) <sup>(1)</sup>	%	NA		≤ 10 (8-12 inch wfrs)	
Off-State power reduction <sup>(2)</sup>			10 X (device)	100 X (device + circuit)	
On-state power reduction <sup>(2)</sup>			4 X (device)	25 X (device + circuit)	
Transistor count			10 <sup>0</sup> - 10 <sup>2</sup>	10 <sup>2</sup> - 10 <sup>4</sup>	10 <sup>4</sup> - 10 <sup>6</sup>
SRAM Yield			NA	100% @ 512Kbits	100% @ 4Mbits

(1) Device metrics must be met simultaneously

(2) Off-State power reduction must be demonstrated by SRAM

(3) On-State power reduction must be demonstrated by ring oscillator



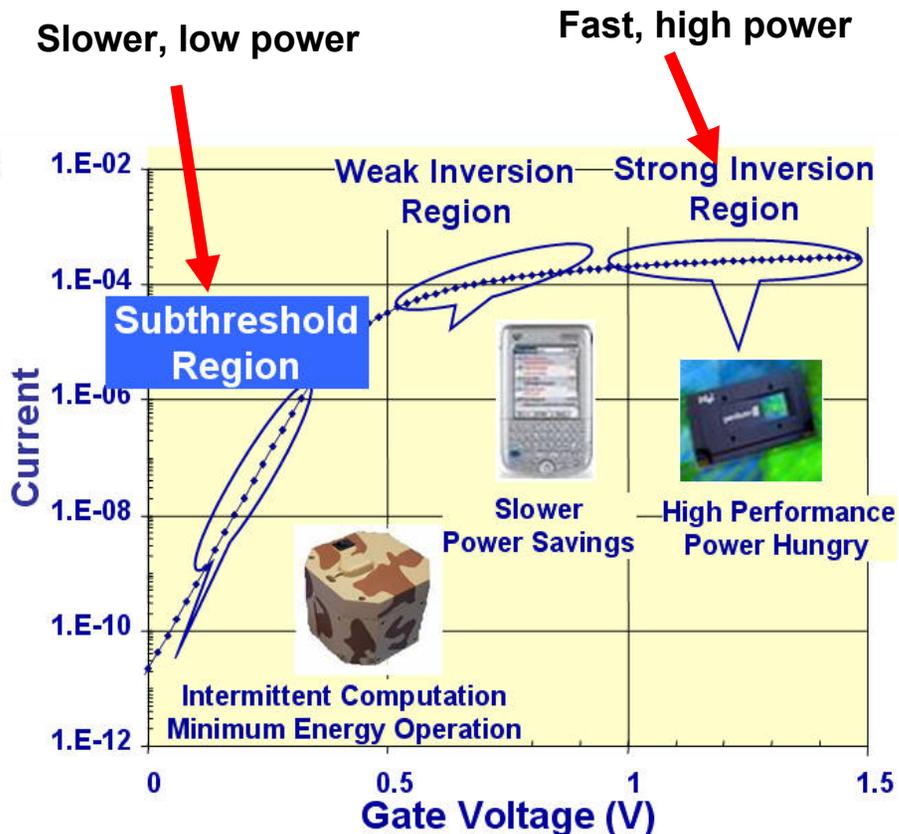
- ESE Program

- “Energy Starved Electronics”

- Create digital ASIC standard cell library working at bias voltages  $\leq 300$  mV (Subthreshold operation)

- No changes to CMOS device technology

- Demonstrate ultra-low power circuit performance



- **Goal:** Enable ultra-low power digital circuits operating in the *sub-threshold regime* while maintaining adequate performance. Power consumption savings > 10X.

### Technical Challenges:

- Develop standard cells operating at  $V_{dd} < 300$  mV; esp. SRAM
- Achieving adequate performance
- Addressing high sensitivity to variations

### Design Only Approach:

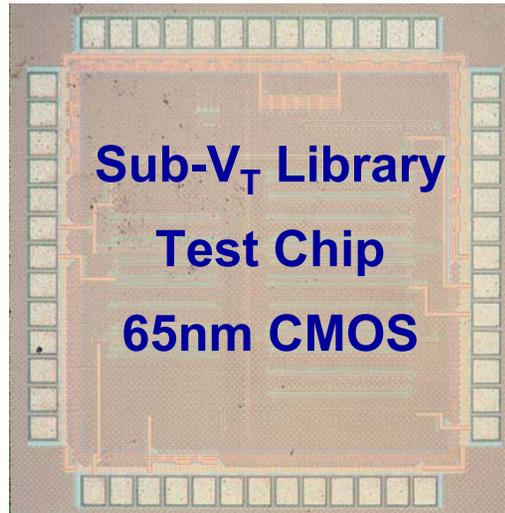
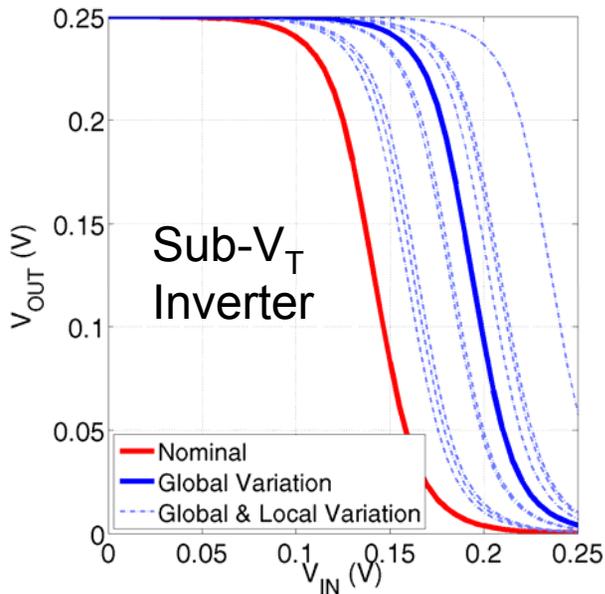
- No device technology changes

### DoD Payoff:

- Autonomous extended operation wireless sensor networks
- Low power portable communications

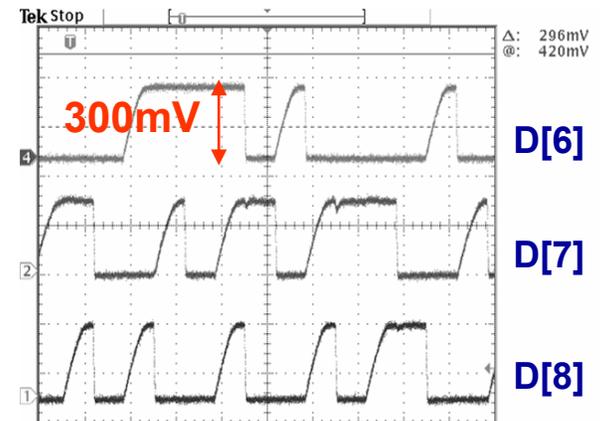
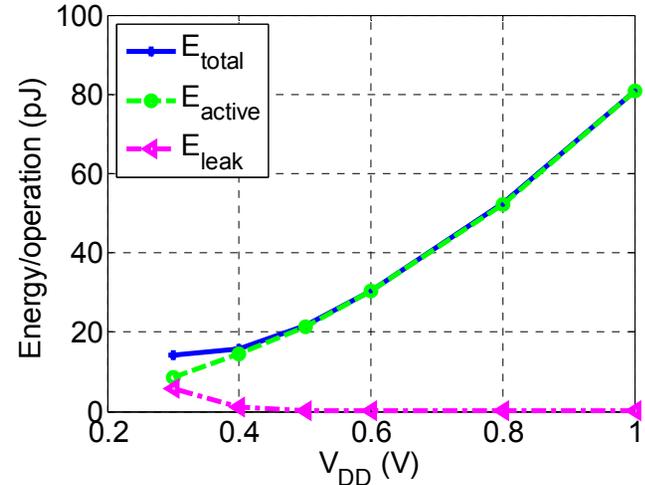
PI: Prof. Anantha Chandrakasan, MIT  
 Fab: TI, Dr. Dennis Buss, 65-nm CMOS

## Goals: Mitigate variation



- Demonstrated a library that operates at  $V_{dd} < 300\text{mV}$
- Includes 62 standard cells

## Enable deep voltage scaling





# Novel Integration Approaches



- **3DIC Program**
  - **“Three-Dimensional Integrated Circuits”**
  - **Develop technologies for integration of multiple active layers in CMOS**
  - **Demonstrate compelling performance/power advantages in 3DIC circuits**

**Interconnect is key bottleneck for power and delay budgets:  
3D solution: Increase bandwidth and lower I/O power**

Tier N

.....

Tier 3

Tier 2

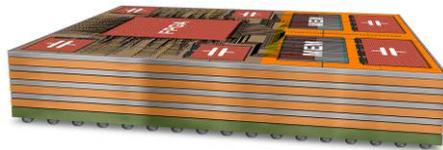
Tier 1



- 1) **High bandwidth between “tiers”**  
Large amounts of cache memory
- 2) **Shorter interconnects**  
High density “area” interconnects
- 3) **Lower I/O power requirements**
- 4) **Novel architectures**  
Performance/Power enhancements



## Stacked-Chips

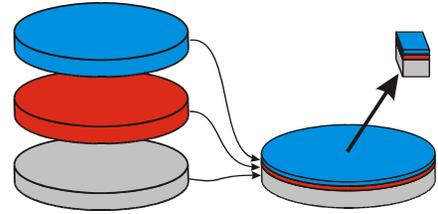


Irvine, RTI

**Circuits-first (die),  
then 3D integration.  
COTS chips possible**

Via:  $30\mu\text{m}/P=100\mu\text{m}$

## Wafer-Scale

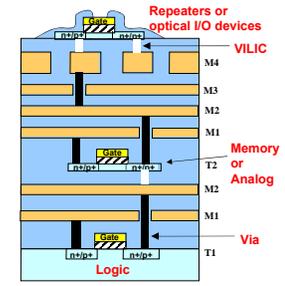


IBM, MITLL, Ziptronix

**Circuits-first (wafers),  
then 3D integration**

Via:  $0.2\mu\text{m}/P\approx 0.4\mu\text{m}$

## Monolithic



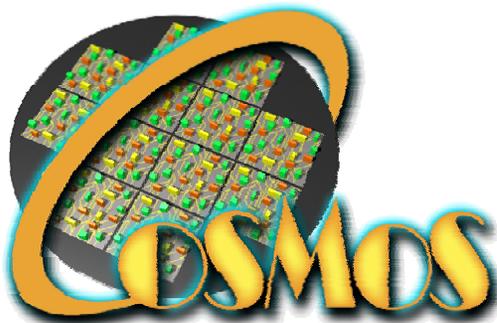
Stanford

**Monolithic 3D  
fabrication**

Via size/pitch (litho limited) 7

- **COSMOS Program**

- **“COMpound Semichenductor Materials On Silicon”**
- **Develop heterogeneous integration technology at the transistor scale**
  - **Compound semiconductor “chipllets” on CMOS wafers**
- **Demonstrate compelling performance advantages in analog circuits**



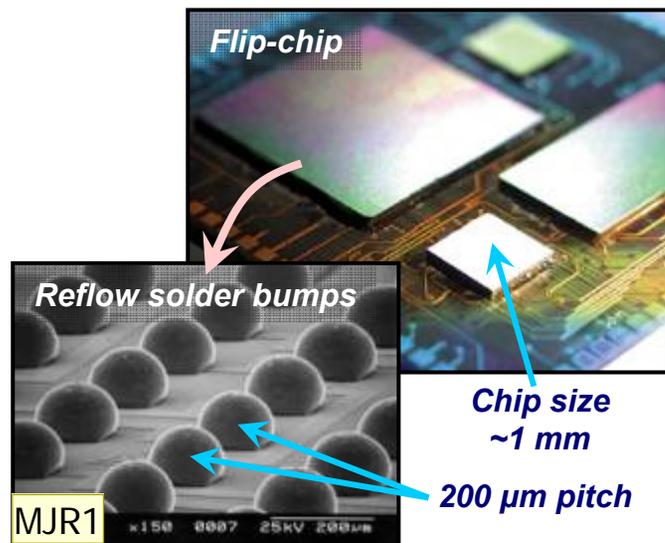
**Program Objective: Heterogeneous integration all the way to the transistor scale**

- Enable **materials selection within circuits** – without loss of transistor performance
- Exploit existing SOA CMOS infrastructure & integration levels – without process modification

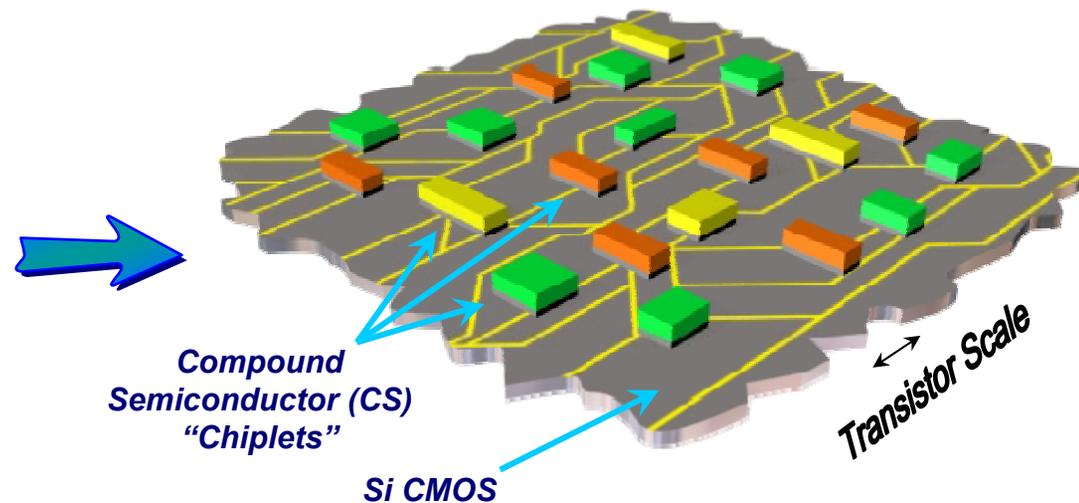
**DoD Benefits**

- Achieve higher functional density: **dense integration of analog, mixed-signal, & digital electronics**
- Enable circuits with lower dissipated power & far higher I/O throughput

**Today**



**COSMOS Vision**



**Heterogeneous integration exists only on a very coarse scale – and not in the signal path**

**Allow the circuit designer to select the optimal transistor technology everywhere in the circuit**

MJR1

Reflowed solder bumps on electroless nickel-gold under bump metal

Mark J. Rosker, 2/5/2006

## Load Transistors

- Highest output impedance to achieve high differential gain
- FOM  $\equiv$  Output impedance

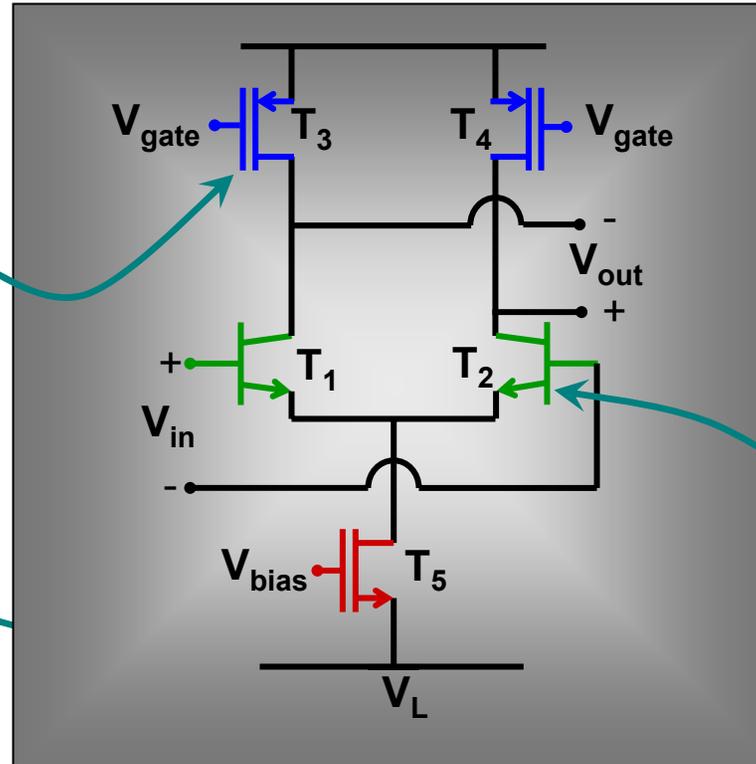
Technology	FOM = $\Omega_{out}$
SiGe PNP HBT	None exists
InP PNP HBT	None exists
Passive Resistor	$\sim 100 \Omega$
Si PMOS	1~1000 k $\Omega$

## Current Source

- Low voltage drop for a given bias current
- FOM  $\equiv$  Voltage across current source (transistor + resistor)

Technology	FOM = $V_{cs}$
ABCS HEMT	$\sim 0.15 V$
Si NMOS	$\sim 0.3 V$
SiGe BiCMOS	$\sim 0.9 V$
InP HBT	$\sim 0.9 V$

## Differential Amplifier



- $\leq 5$  transistors with markedly differing characteristics
  - High open-loop gain
  - High speed; large voltage swing
  - Low power consumption
- Core circuit building block common to all ADC architectures
  - Fundamental to comparator
  - Op-amps, cascode amps, and many other amplifiers are based on this DA

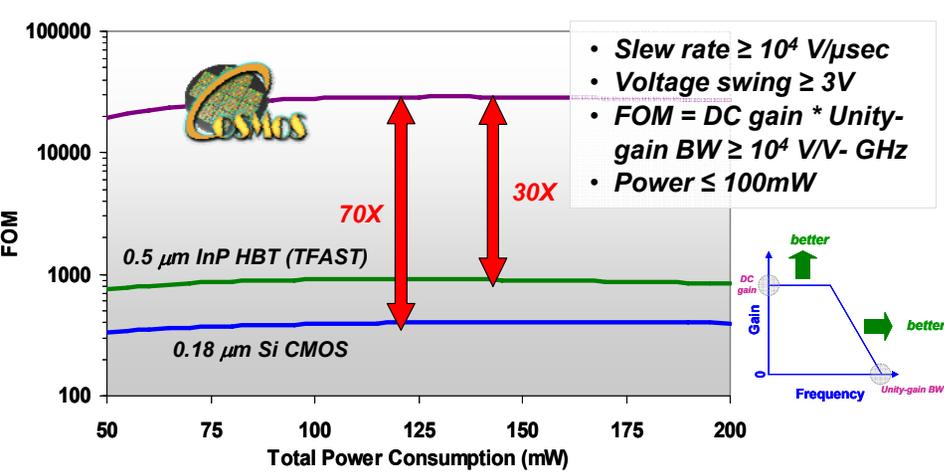
## Differential Pair

- Highest speed and largest voltage swing to achieve high slew rate
- FOM  $\equiv f_t * BV$

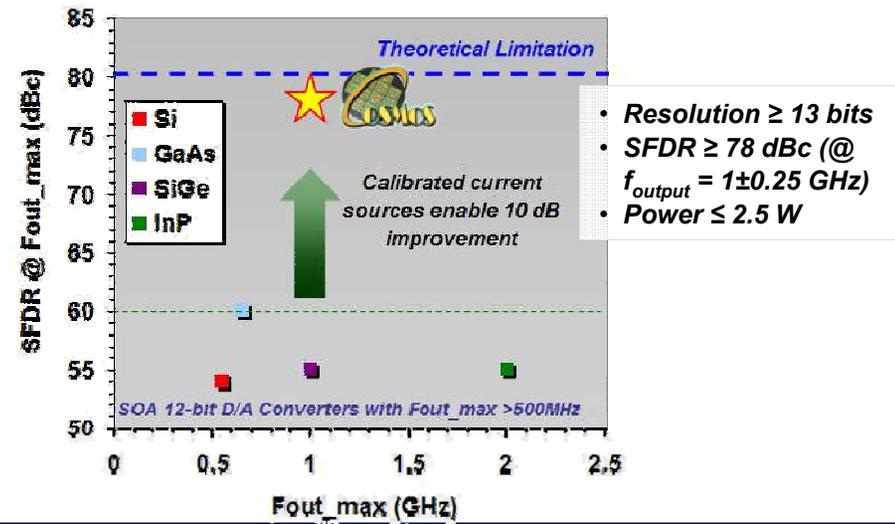
Technology	FOM = $f_t * BV$
SiGe NPN HBT	350 GHz-V
Si NMOS	600 GHz-V
GaN FET	1000 GHz-V
InP NPN HBT	2400 GHz-V

**COSMOS allows the choice of the best transistor for each function**

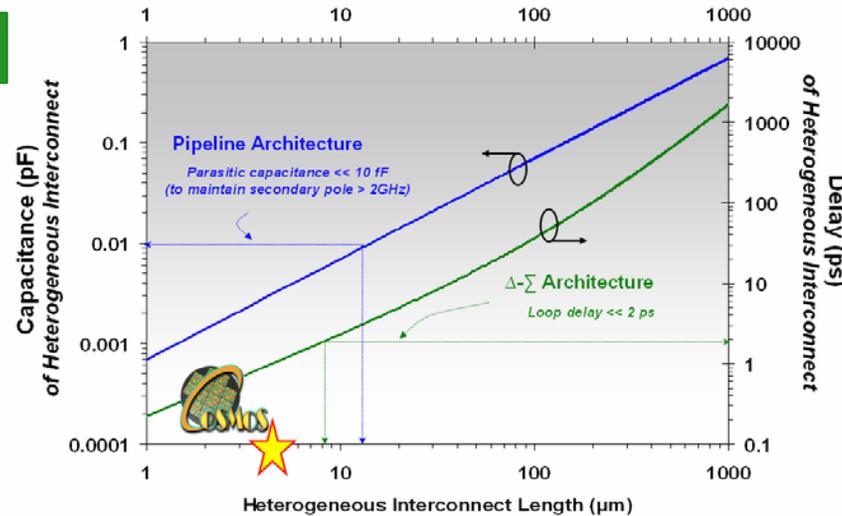
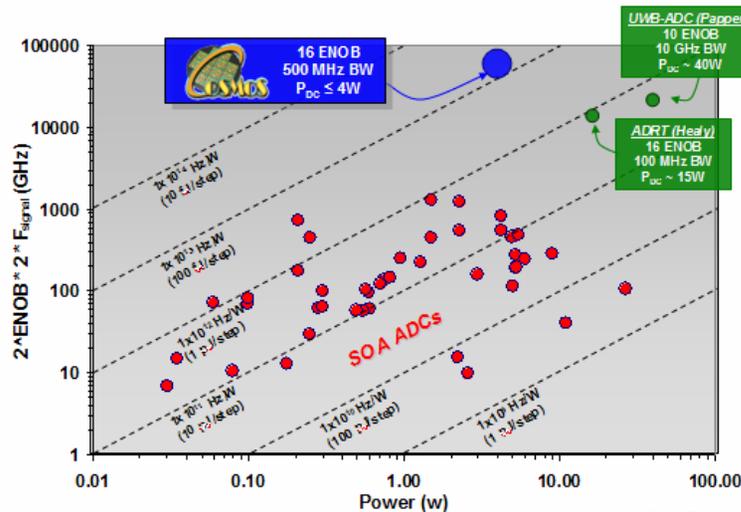
## Phase I: Differential Amplifier



## Phase II: D/A Converter



## Phase III: A/D Converter



- 16 SNR bits
- 500MHz BW
- SFDR  $\geq 98$  dBc
- Power  $\leq 4$ W