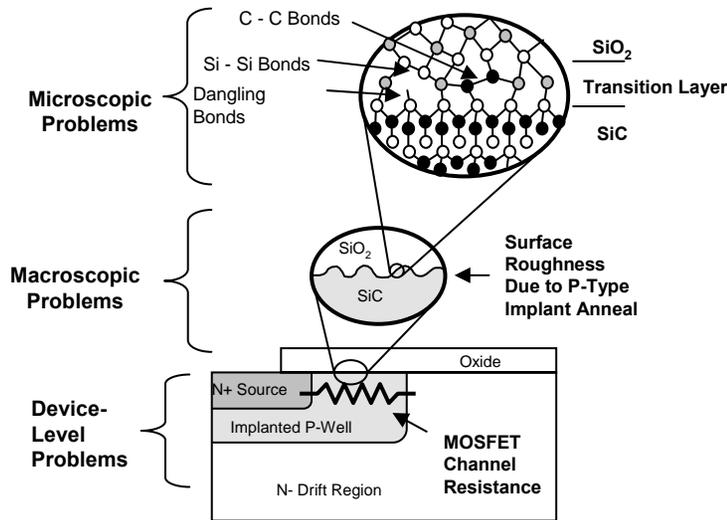


# Development of Process Technologies for High-Performance MOS-Based SiC Power Switching Devices

Purdue, Auburn, Vanderbilt, Carnegie Mellon, Oak Ridge National Labs, Dow Corning



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## Goals, Objectives and Main Technical Approach

- Improve the **surface morphology** of the SiO<sub>2</sub>/SiC interface in implanted regions using low-damage implantation techniques and silane annealing.
- Reduce the density of **MOS interface states** on 4H-SiC by optimizing the oxidation and anneal procedures. Particular emphasis is placed on passivation by nitrogen and hydrogen using post-oxidation annealing in NO and NO+H<sub>2</sub>. Deposited oxides and a-axis surfaces will also be investigated.
- Optimize **edge terminations** to achieve high blocking voltage. Floating field rings and three-zone JTE will be investigated using numerical simulations and experimental PiN diodes.
- Grow **thick epilayers** necessary for 10 kV power devices using an Epigress VP-508 CVD reactor.
- Develop **10 kV SiC UMOSFETs** using the trench-oxide-protection (TOP) structure, combined with optimized edge terminations.

## Key Accomplishments

- Significantly improved surface morphology over implanted p-wells in 4H-SiC DMOSFETs using silane ambient annealing (Capano)
- Increased MOS channel mobility in 4H-SiC to **60-70 cm<sup>2</sup>/Vs** using NO +H<sub>2</sub> post-oxidation annealing (Williams and Feldman)
- Reduced MOS channel resistance in implanted DMOSFETs to **< 10 mΩ cm<sup>2</sup>** using a combination of NO post-oxidation annealing, silane implant annealing, and a novel self-aligned short-channel process (Cooper)
- Optimized JTE and FFR edge terminations by computer simulations, obtaining **BV ≥ 80%** of the theoretical plane-junction value (Cooper)
- Grew very thick (**>200 μm**) n-type epilayers capable of BV > 20 kV using the Epigress VP-508 hot-well CVD reactor (Capano)
- Fabricated trench-oxide-protected (TOP) UMOSFETs on 115 μm epilayers with **R<sub>ON,SP</sub> ≈ 240 mΩ cm<sup>2</sup>** (Cooper)
- Developed **new concepts** for very-high-voltage (>20 kV) MOS power devices

## Major Impact of Technology & Technology Transition Plan

- The improved surface morphology of the SiO<sub>2</sub>/SiC interface in implanted regions and the reduced density of MOS interface states will increase inversion layer mobility in SiC power MOSFETs, **reducing the specific on-resistance and improving system efficiency.**
- Optimized edge terminations will **increase the blocking voltage** of high-voltage SiC power devices without increasing the on-resistance, thereby bringing these devices closer to the theoretical performance.
- The ability to grow thick epilayers at controlled doping in the Epigress VP-508 reactor will provide an **improved understanding** of factors governing epitaxy for high-voltage SiC power devices.
- Demonstration of 10 kV SiC UMOSFETs using the trench-oxide-protection and optimized edge terminations will provide a path toward **megawatt power devices** needed for DoD applications.
- Design and processing technology has been transferred to other contractors under the DARPA WBG HPE program.