Microsystems Technology Office

Dr. Robert Reuss

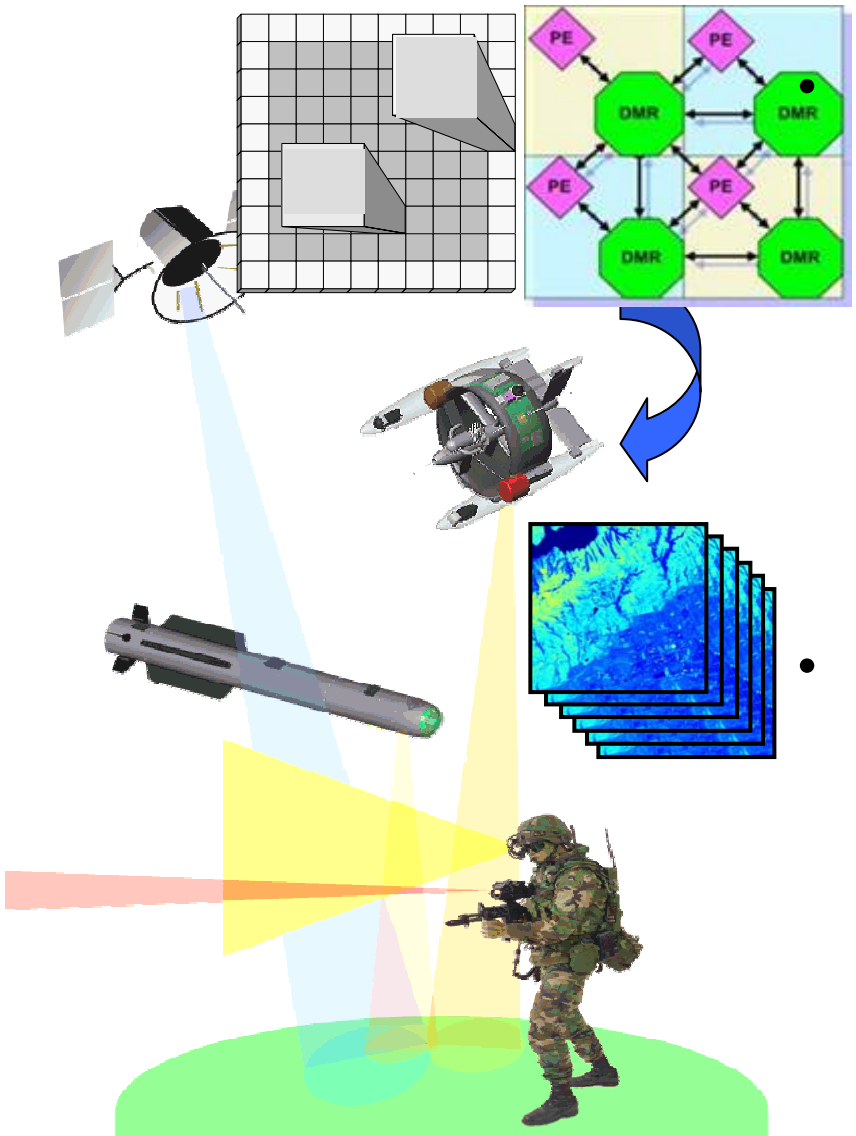
Approved for Public Release, Distribution Unlimited

Embedded Configurable High Performance Processing of Signals

ECHiPPS

Program Manager, Robert Reuss

Embedded Configurable High Performance Processing of Signals (ECHiPPS)



Goals

- High performance signal processing at significantly lower power in a reconfigurable architecture to enable new missions which require low-power, adaptable, high performance embedded processing not available today.
- Demonstration of prototype chip performance in DoD relevant applications.
- Software tools for implementation of military applications.

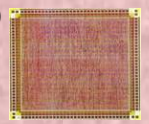
Technical Challenges

- An order of magnitude (10x) increase in both power and throughput performance over the current state-of-the-art reconfigurable (FPGA) and general programmable processors.
- Chip design and fabrication of an adaptable-reconfigurable integrated circuit consisting of repeatable units of processing elements and memory communicating thru a unique on-chip network architecture.
- Integrated hardware/software development environment for design ease by non-experts.

What is Embedded Configurable High Performance Processing of Signals (ECHiPPS)?

- ASICs are far too costly to implement.
- μ–procs, PCA or FPGAs can't meet many high performance embedded mission requirements.

ASICS: Point solutions to specific problem set.



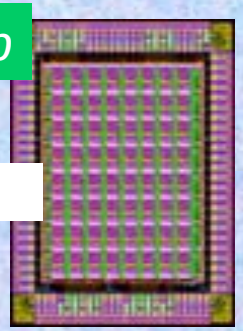
Full Custom ASIC

~10 pJ/op

Standard Cell ASIC

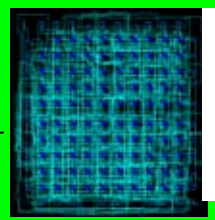
Reconfigurable Processors: Wider range of solutions.

~500 pJ/op



FPGA

ECHiPPS



- ✓ ASIC-like performance.
- ✓ Flexibility/cost of reconfigurable proc.

better than 10 pJ/op

μProcessors COTS DSPs

Programmable. Used when performance is not critical.

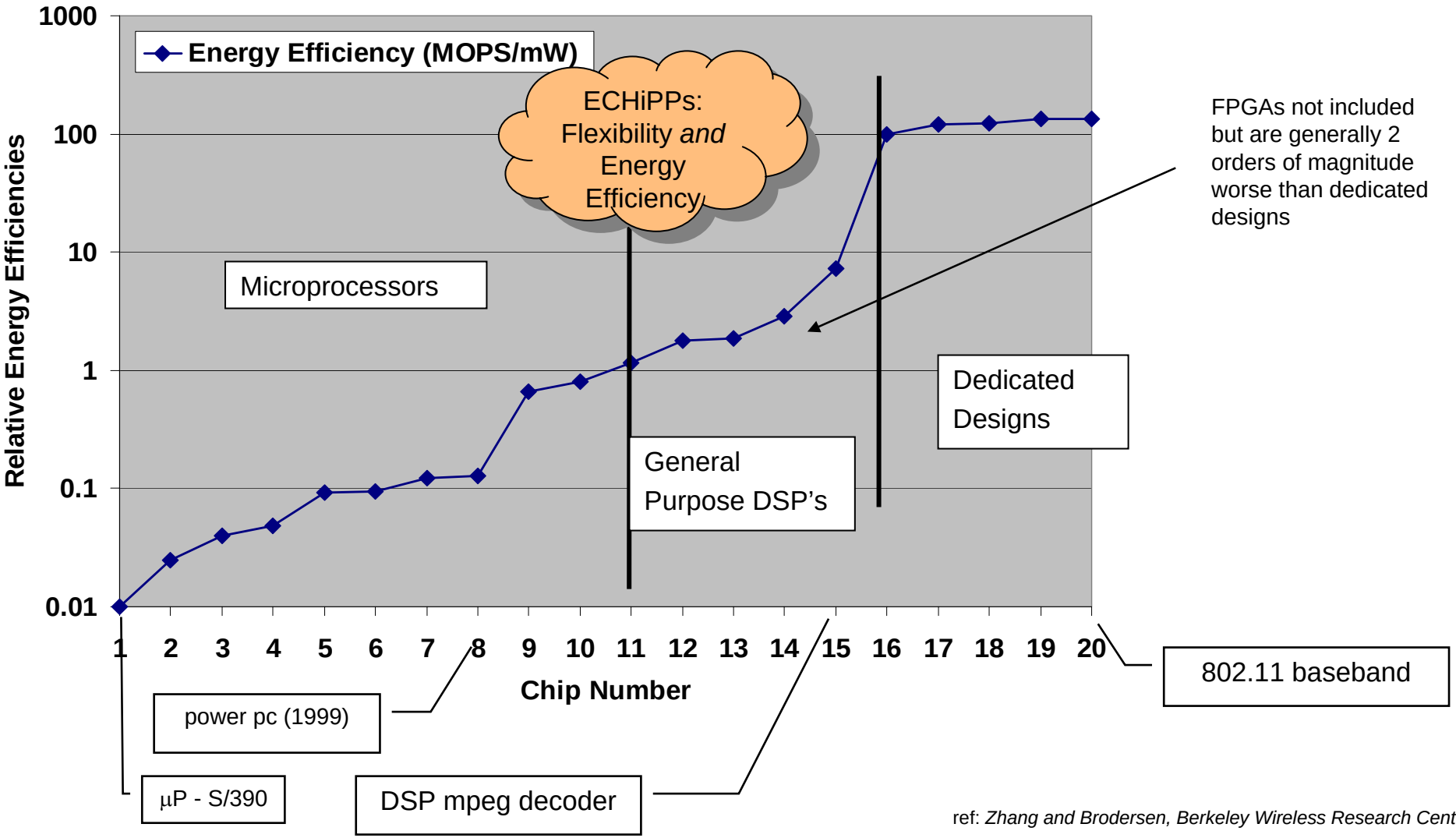
10,000 pJ/op

Embedded, Real Time, Power Constrained Applications

Implementation Costs (time and $$,)

Requirements (Higher Performance, Less Power)

ECHiPPS Technical Challenge: Greater Flexibility Can Result in Lower Energy Efficiency



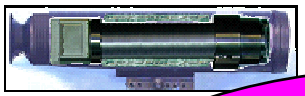
ref: *Zhang and Brodersen, Berkeley Wireless Research Center*

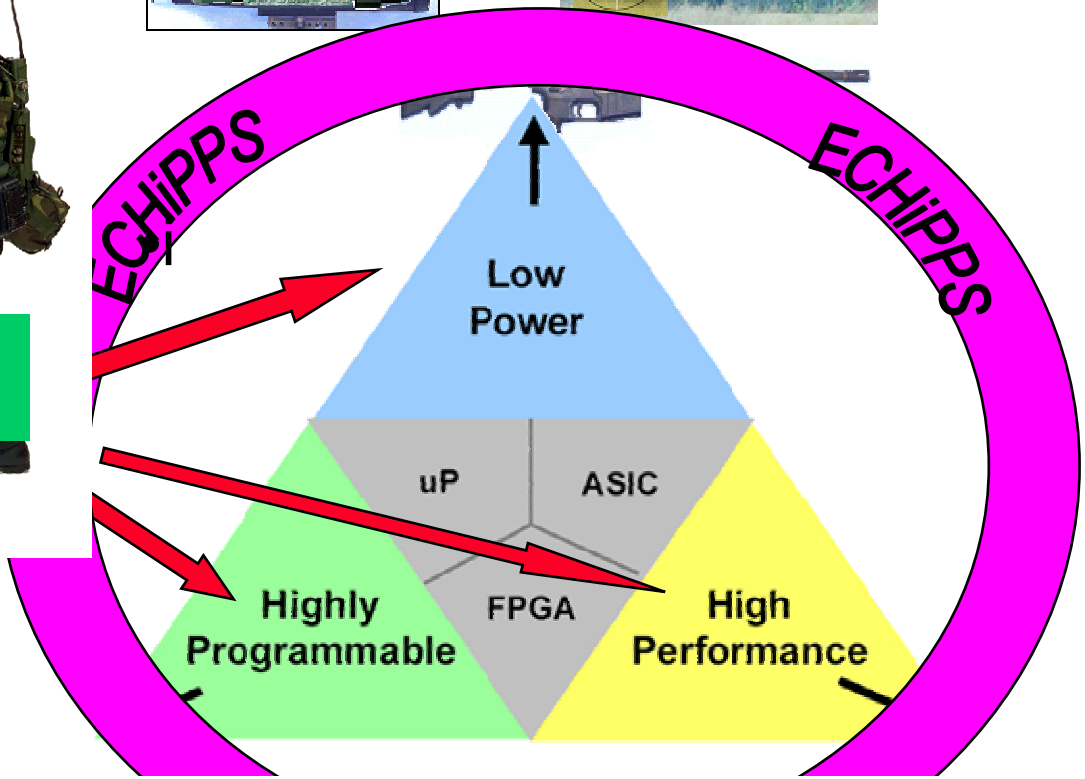
ECHiPPS: Configurability AND Performance.

- Commericial IC marketplace forces choice between flexibility and performance.
- **DoD embedded processing programs**, such as those running on battery power or with changing missions **require both**.

Unique Functionality

Application Requirements





Trade-off Space for Processor Technologies

ECHiPPS

ECHiPPS goal: enable critical military applications that are constrained by current limitations of embedded processors.

- Power –less than 5 watts
- ASIC-like Performance
- Reconfiguration – do not need new chip if mission parameters change.

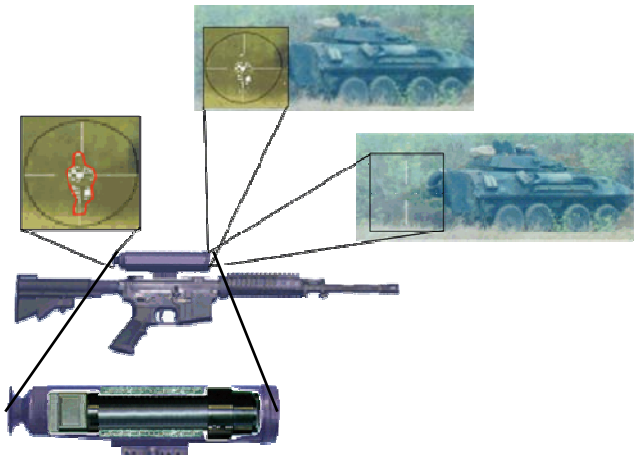
ECHiPPS: Addressing DoD Need Power Efficient Embedded Chip Performance

Individual Warfighter

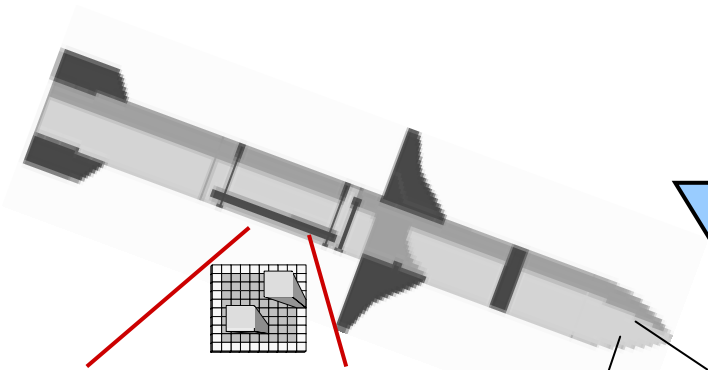
ECHiPPS program goal is to <u>enables critical military applications</u> that are constrained by current limitations of embedded processors.

- Power –less than 2 watts
- ASIC-like Performance
- Reconfiguration – do not need new chip if mission parameters change.

Missile Seekers

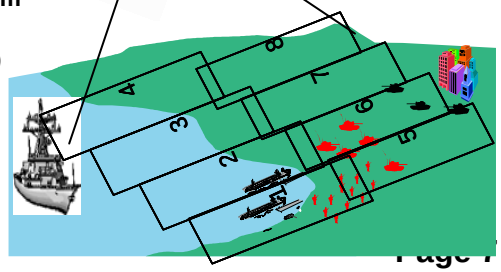


HyperSpectral Gun/Helmet Scope Image Fusion

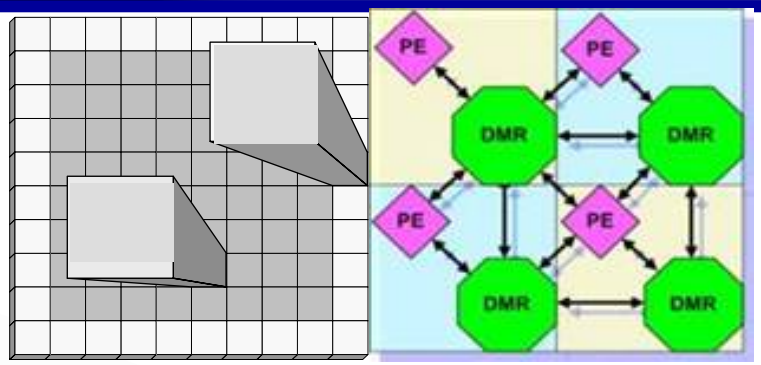


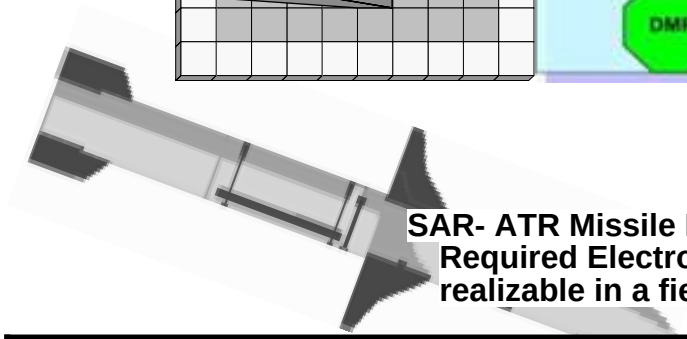
SARATR Missile Platform
Current Electronics Not Realizable in a Field System
Current Implementation
Processors > 40 PowerPC 7410s (Mercury/Race++)
Power > 400 W

Radar



ECHiPPS Prototype Reconfigurable Processor





SAR- ATR Missile Platform
Required Electronics not currently realizable in a field system

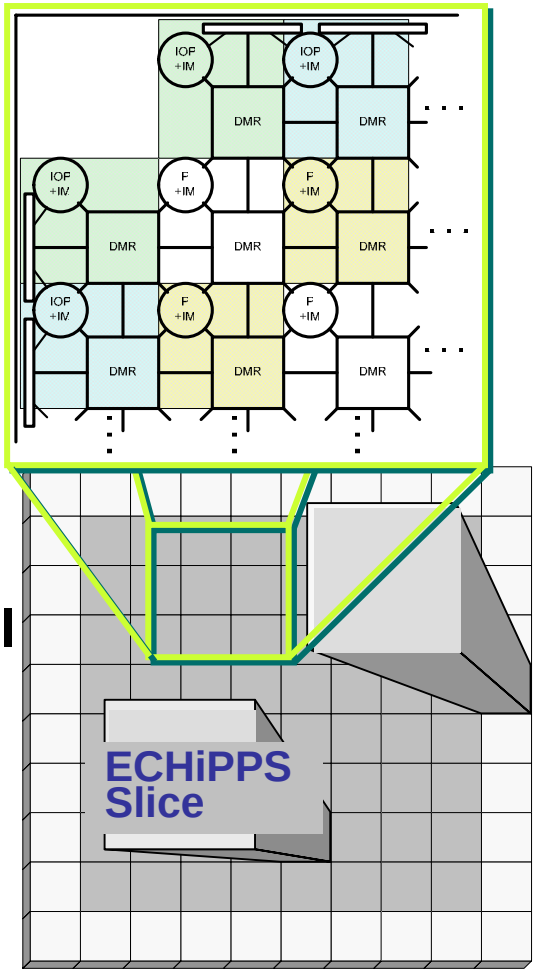
Implementation	Peak Power(W)	Efficiency (msec per image)	Energy Efficiency (W*sec)
ECHiPPS	.96	4.38	.00420
Actual SAR platform (30 PowerPCs)	141	2000	282
PowerPC platform matching ECHiPPS throughput (128 PowerPCs)	601.6	4.894	2.94423

- **Goal:**
  - High performance signal processing at significantly lower power in a reconfigurable architecture
- **Technical Challenges**
  - Chip design and fabrication of the adaptable-reconfigurable integrated circuit consisting of repeatable units of processing elements and memory.
  - Integrated hardware/software development environment.
- **Key Accomplishments**
  - SAR analysis was performed. Results show ECHiPPS processor can achieve orders of magnitude reduction in both performance and energy.
- **Impact**
  - ECHiPPS processor enables new missions ensuring U.S. technological dominance over adversaries in situations requiring low-power, adaptable, high performance in-the-field processing.

Approved for Public Release, Distribution Unlimited

The ECHiPPS Approach
A Balanced Architecture

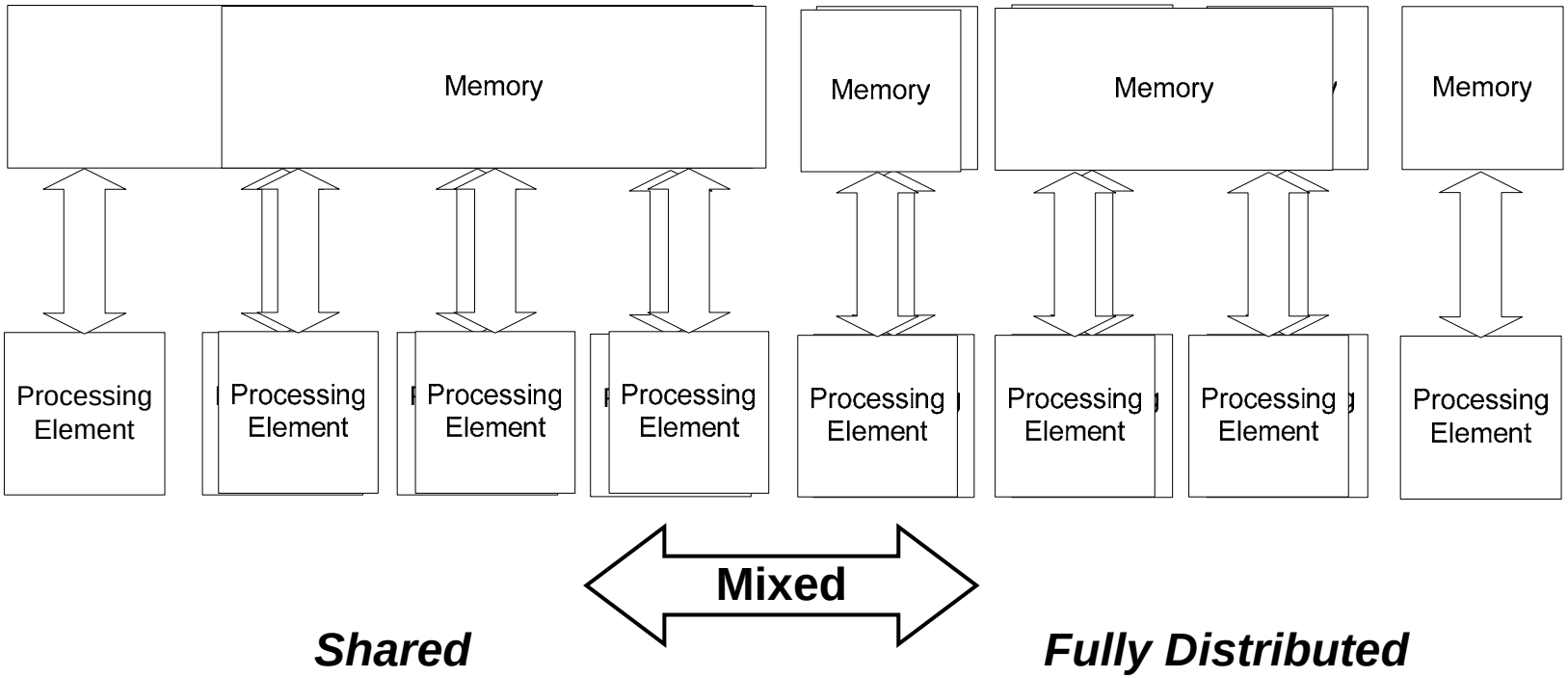
- **ECHiPPS Slice**
  - **Processing Element**
    - 500 MMACS @ 500 MHz @ 16-bits
    - 1 BMACS @ 500 MHz @ 8-bits
  - **DMR**
    - Communication / On-Chip Network
      - **Topology Independent**
      - **Sustain > 4 GBytes per second of data transfer**
      - **Provides multi-dimensional data movement**
        - Nearest neighbor, regional, and global
    - Memory: addressed data and instruction memories
      - **Mixed Programming Memory Model**
- **IO**
  - **Programmable IO structure**
    - Follows HyperSlice architecture
    - Seamless expansion of the architecture across multiple HyperX chips
      - **Massively parallel solutions are feasible (tens of thousands of processors)**
    - Provides seamless boundary to external interfaces
      - **DDR memory, parallel, serial, A/D interfaces, different clock rates**



ECHiPPS Processor

Approved for Public Release, Distribution Unlimited

ECHiPPS Architecture
Incorporating Both Shared and Distributed Memory Model



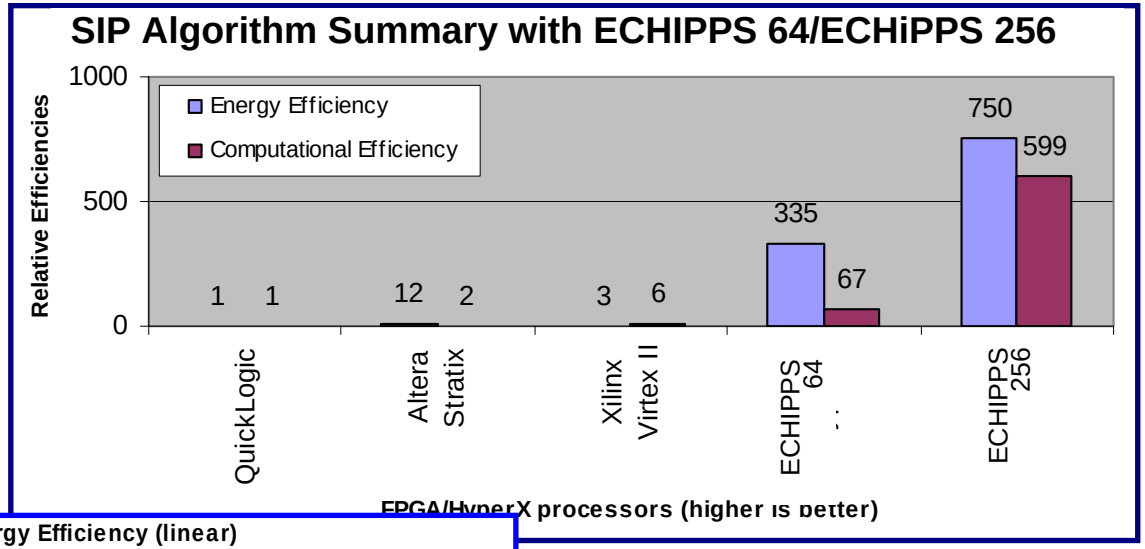
Abstract Programming Memory Model

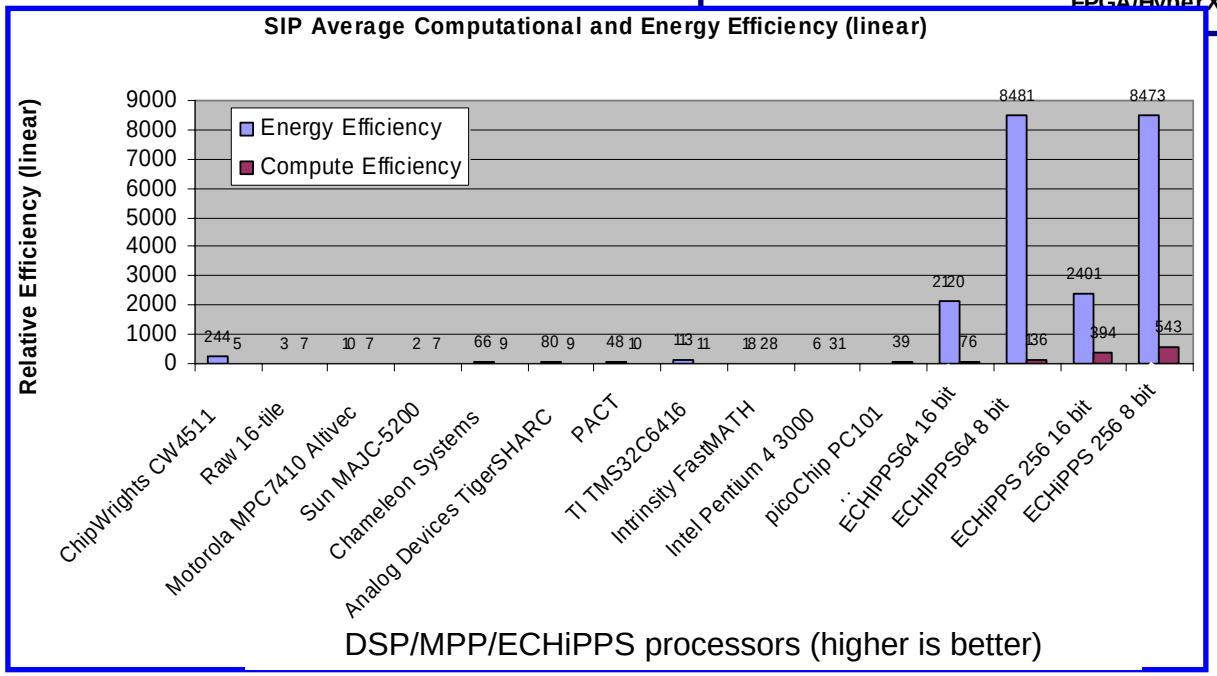
Approved for Public Release, Distribution Unlimited

ECHiPPS Simulated Algorithm Demonstration

- **Computational Efficiency**
  - **Better than 10X**
- **Energy Efficiency**
  - **Better than 100X**

vs. FPGA & DSP/MPP Technology





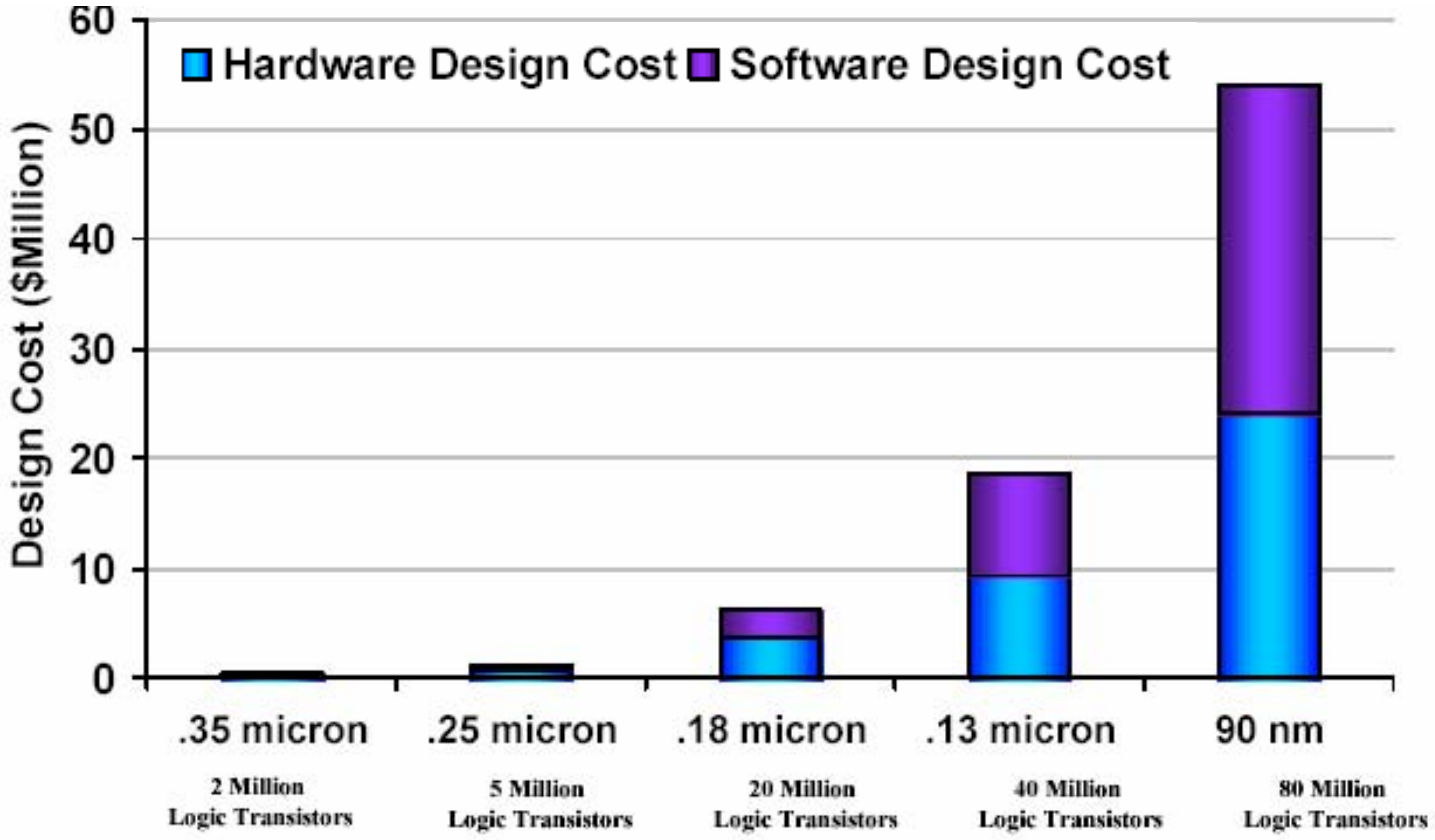
- **Signal & Image Processing (SIP) Algorithms**
  - **FFT**
  - **Convolution & FIR**
  - **Scalar Multiplication**
  - **Translation & Rotation**
  - **Matrix Multiplication**
  - **Gaussian Elimination**

Approved for Public Release, Distribution Unlimited

ECHiPPS Including Software Tools

IC design costs are prohibiting future military capabilities.

- ECHiPPS solutions will drastically reduce hw design and sw design costs for ASIC-like performance.
- Solution specifically aimed at low power, signal processing applications.



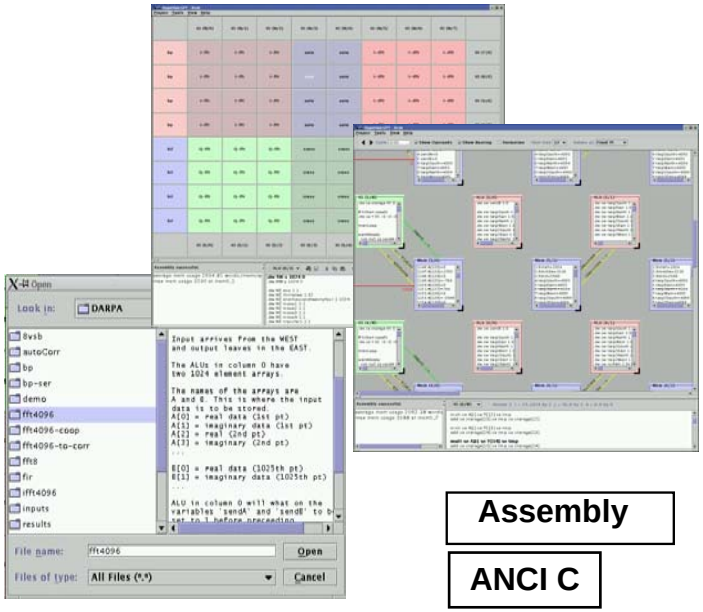
Source: IBS, Analysis of the Relationship Between EDA Expenditures and Competitive Positioning of IC Vendors

Tool Development

Supporting Algorithm to Hardware Implementations

Spatial and Temporal Programming Environment

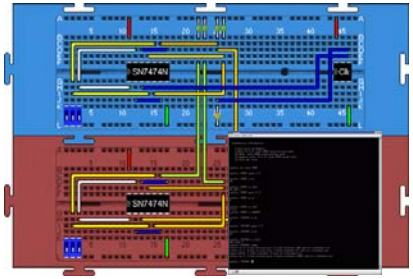
- **High-Level System/Algorithm Development Environment**
  - e.g. The Mathworks' Simulink, Mathematica, Elanix's SystemView, C/C++



Assembly

ANCI C

The ECHiPPS Program



Cycle Accurate Chip Simulator

ECHiPPS Hardware

Approved for Public Release, Distribution Unlimited