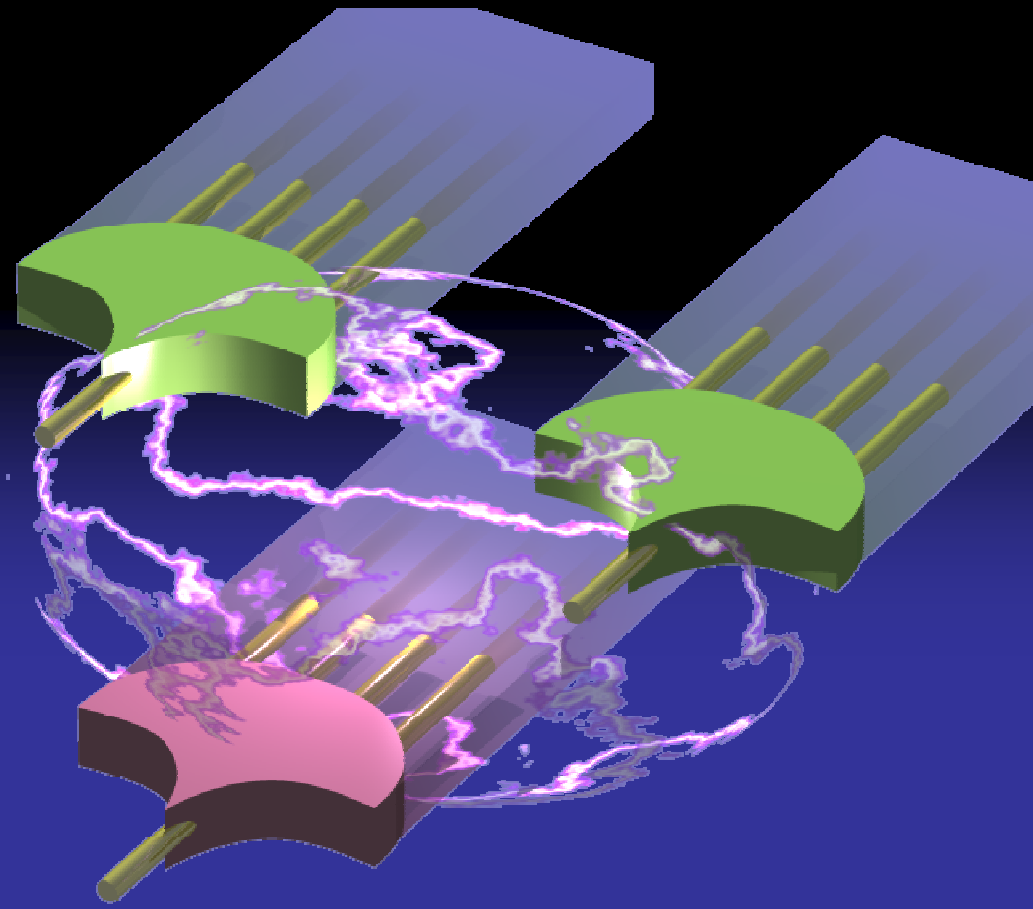
Clockless Logic, Analysis, Synthesis and Systems

The CLASS Program



Dr. Robert Reuss
Program Manager

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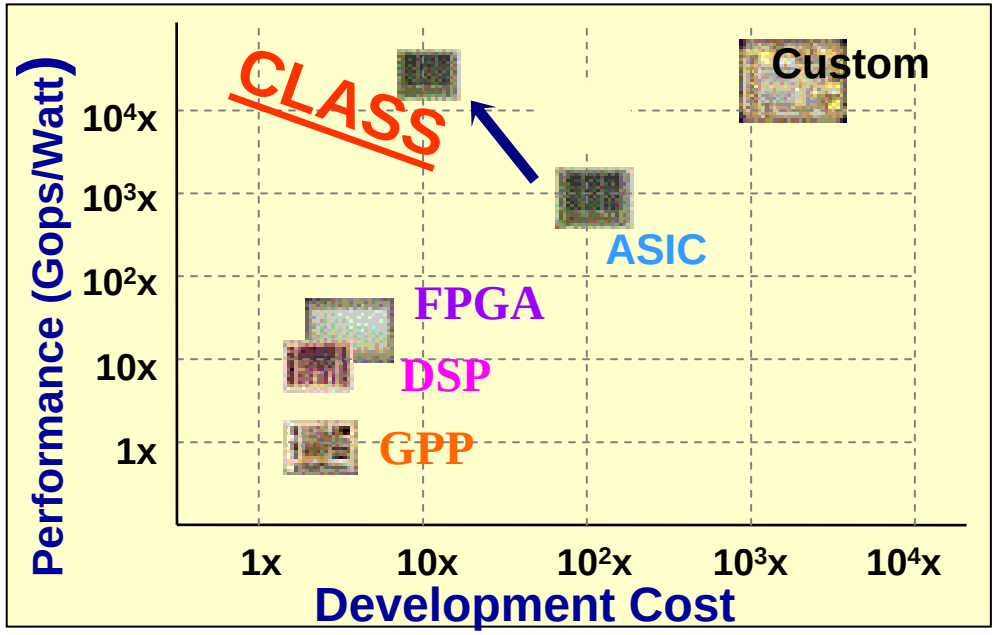
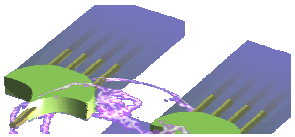


CLASS Program Goals:

- Demonstration of the cost and performance advantages of asynchronous/clockless integrated circuit design.
- Overcome clocked design inertia and enable automated design of clockless circuits.
- Make clockless design available ASAP to DoD.



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Goals

- Enable design of clockless circuits.
- Overcome clocked design inertia
- Make clockless design available ASAP to DoD.

Approach

- Develop Clockless Simulation, Synthesis & Libraries with Commercial EDA Tools
- Expand Industry Involvement in CLASS Program
- Demonstrate clockless design in complex, highly-constrained, DoD system.
- Technology Transfer

Asynchronous Design Revolution Was Not Required in Pre Nano Electronics - <u>but Now Overdue</u>

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CLASS Tools Reduce Need for Clockless Expertise

Design before CLASS

Best of Breed Solutions

–Develop missing enabling tools - make user friendly

–Provide diverse technology for spectrum of requirements

Technology Transfer

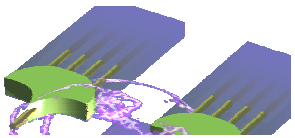
–Supported by commercial companies

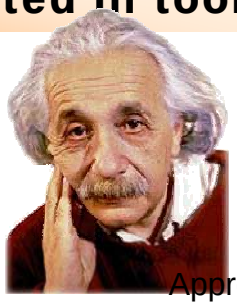
–Seamless invisible integration

–Publish and Educate

Expert Tool

Expert knowledge incorporated in tool





Enables average engineer to successfully implement asynchronous design with standard tool flow

CLASS

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Why Clockless?

Clockless technology will enable very vomplex SoC designs by overcoming approaching limits of clocked design

- **Timing Closure**
- **Noise/EMI**
- **IP Reuse**
- **Power Management**
- **Limited Available EDA Tools**
- **Device Variation**

• Multi-rate behavior

Circuits are data driven not clock driven. Local handshaking.

• Low Noise and Low EMI

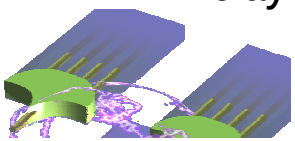
The lack of synchronized switching spreads the demand on the power rails over the frequency spectrum

• Power Management

The circuits are data driven and only consume power when doing useful work
Match power supply to required data rate
Low latency recovery from sleep mode

• Delay Insensitive

Agility and reconfigurability enabled with no timing closure issues to break the functionality
Higher levels of integration by simple accretion
Designs easily ported to new materials and run at the speed enabled by the new technology

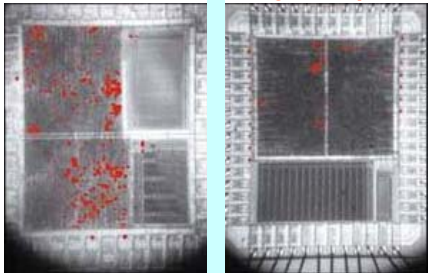


Advantages of Clockless Design

Power

- Appropriate design maximizes power savings by eliminating clock and minimizing power for handshaking
- Clockless design auto power manages

Red indicates high temp

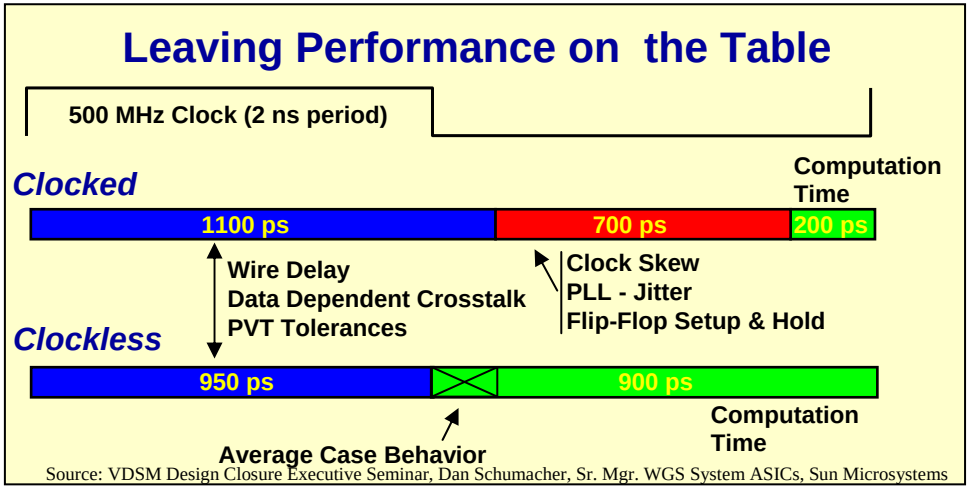


Potential Power Benefits Demonstrated by Intel RAPPID, Theseus NCL08 and NCL8051, Cogency DSP/ADC, and other clockless implementations

Performance

- Eliminates timing closure or performance killing margins
- Auto micro pipelining

Potential Performance Benefits Demonstrated by Intel RAPPID



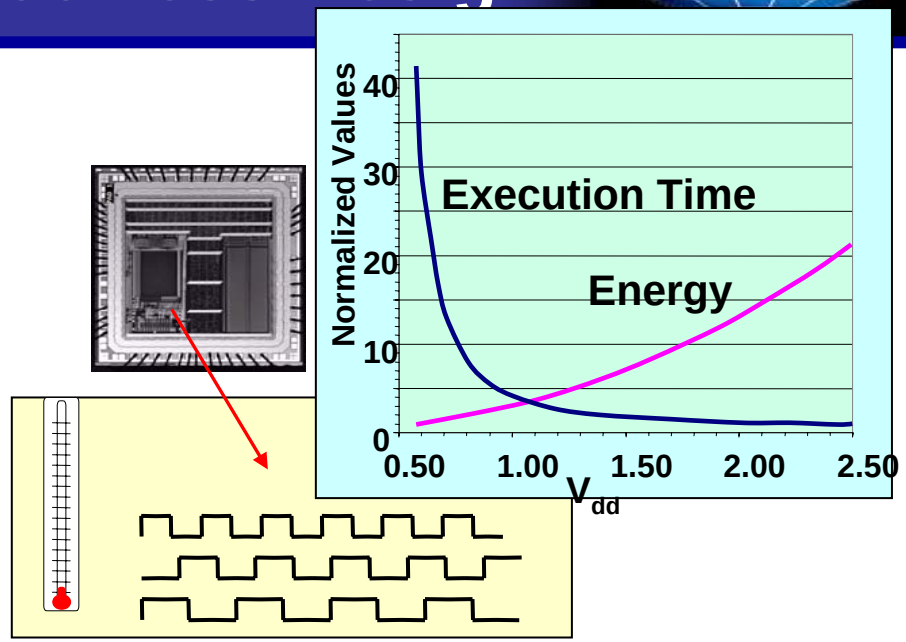
32-bit Adder

Advantages of Clockless Design

Wide Operating Conditions

Tolerant to device variations and environmental variations

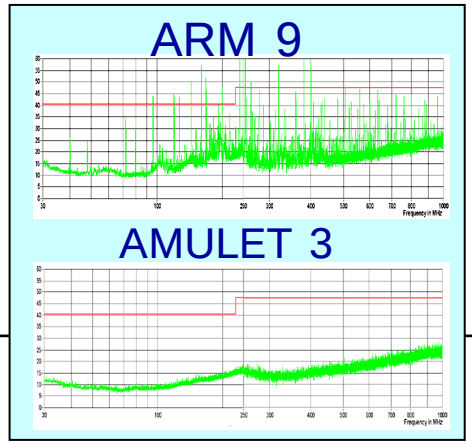
Potential Benefits Demonstrated by Theseus NCL08 operating to extreme low voltage



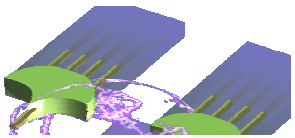
Interference

- Reduces substrate and power rail noise
- Improved Analog and RF performance

Reduced interference demonstrated by Amulet and Cogency DSP/ADC Clockless Circuits

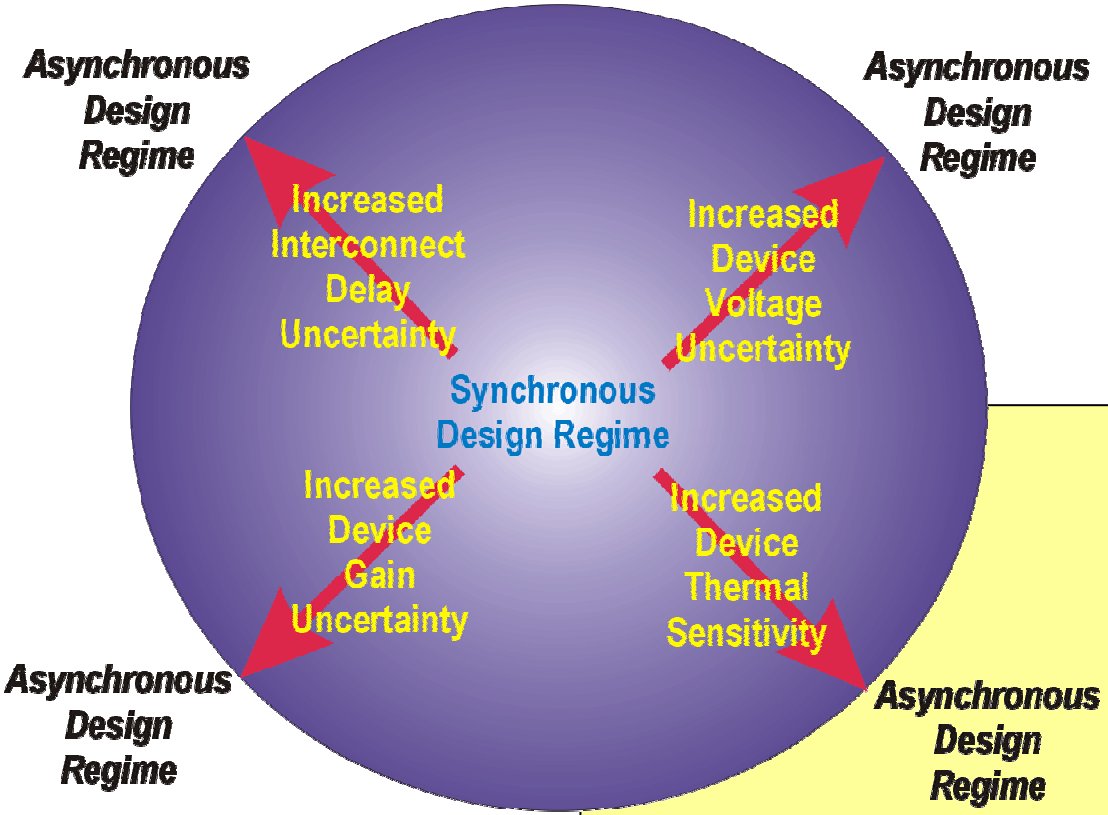


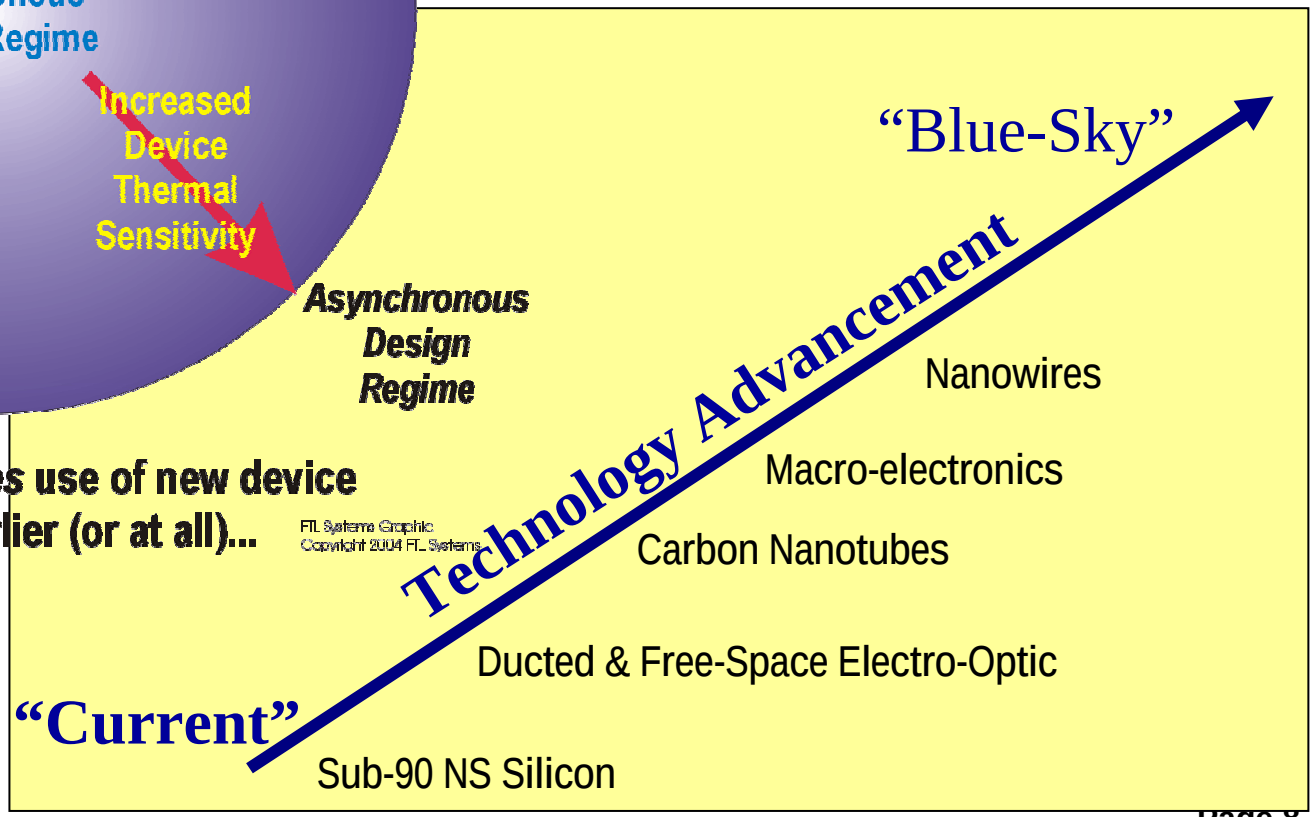
Easier Re-use of IP



- No global clock effects that span IP
- Flexible Interfaces

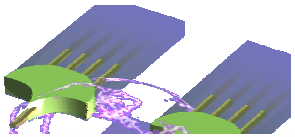
Clockless Technology Enables Use of New Device Technologies





Asynchronous design *enables* use of new device technologies generations earlier (or at all)...

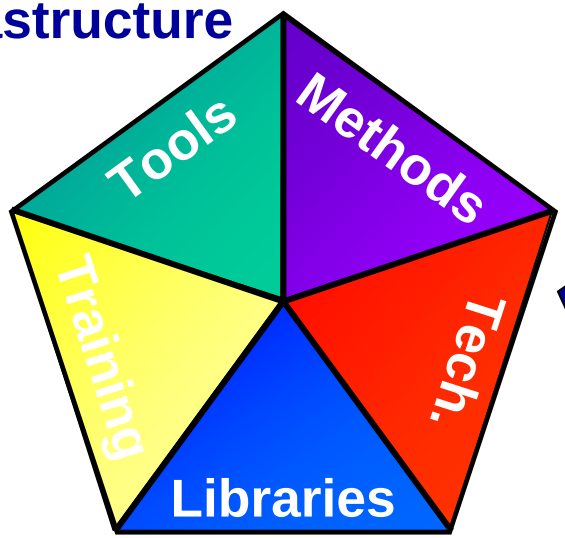
FTL Systems Graphic
Copyright 2004 FTL Systems



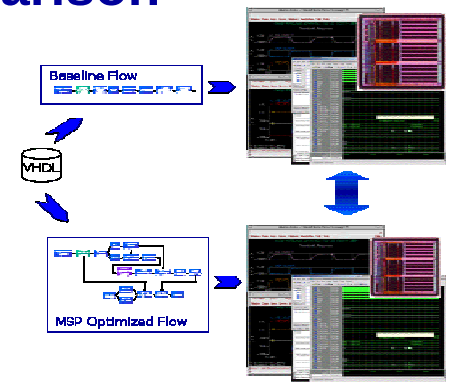
CLASS

Key Products for CLASS

Clockless Design Infrastructure



A vs. B vs. C Comparison



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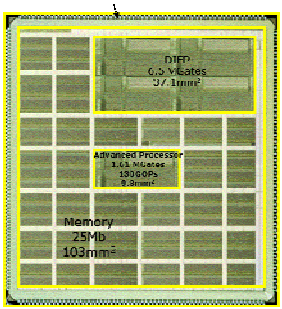
Asynchronous Advanced Sensor Processor ASIC

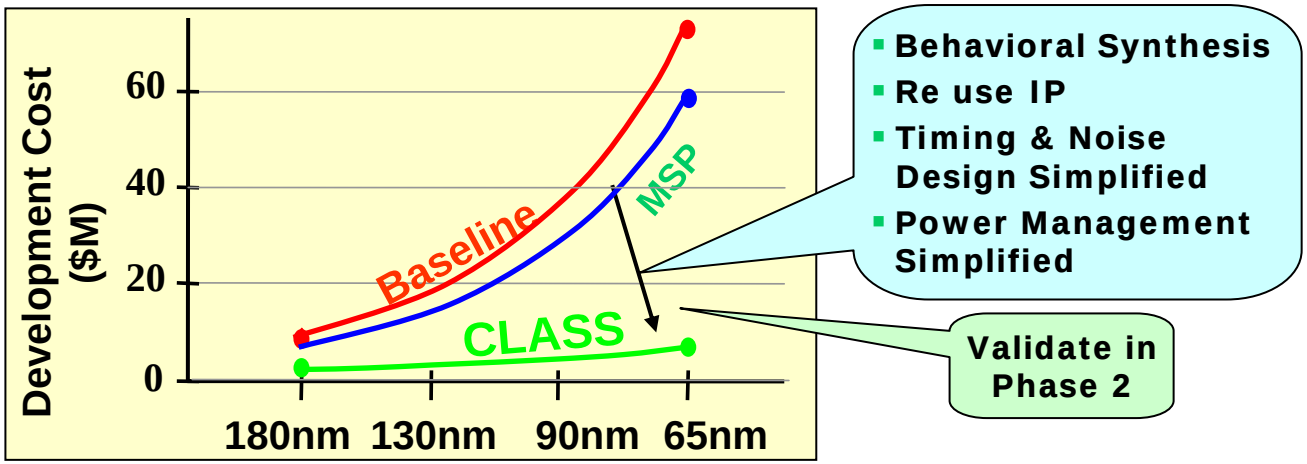


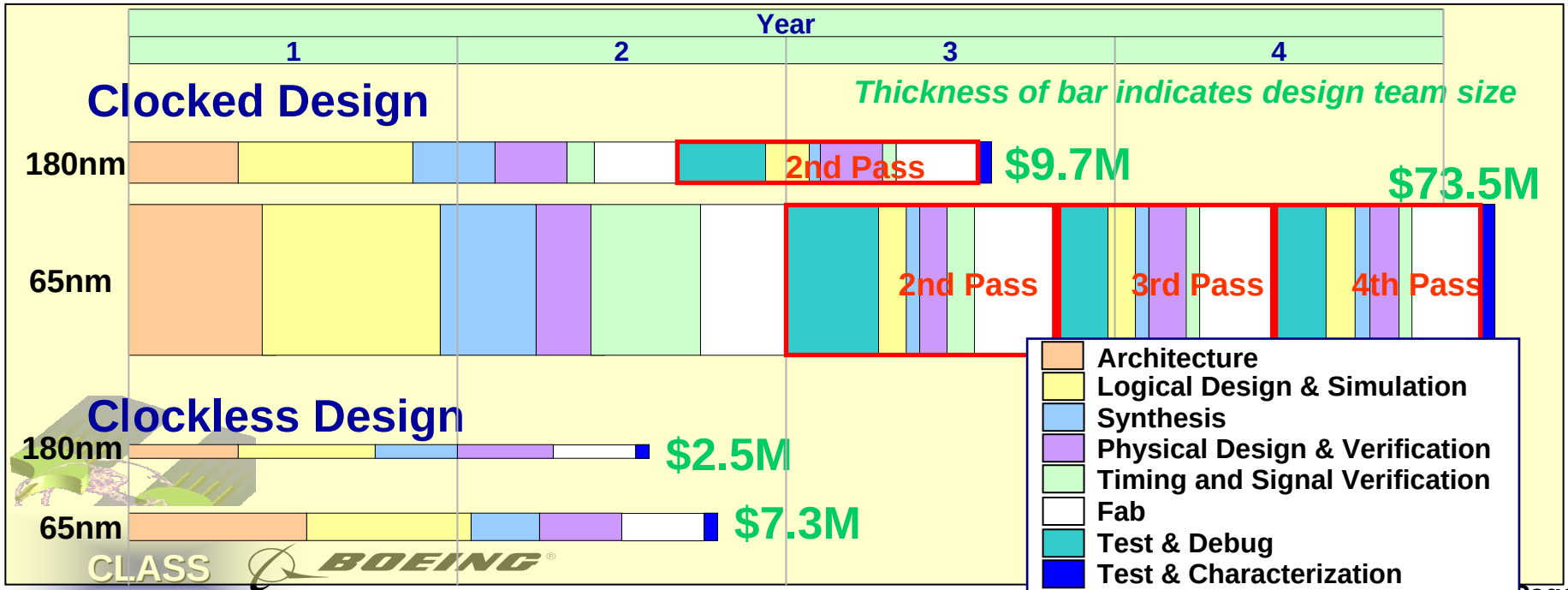
Real-time Demonstration

CLASS to Make SoC Affordable

Assumptions

- Complex, High-Performance, Digital SOC
- Designed without excessive timing margins





CLASS Program Description

Objective

Establish Clockless Design Infrastructure →

Push Clockless Design Into Mainstream →

Approach

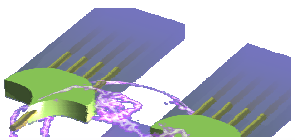
Develop Robust CAD Environment
- RTL to GDSII
- Commercially Available & Supported
- IP
- Proven

Provide Significant Advantage Over Traditional Designs
- Performance
- Power
- Design Time
- Integration
- Security

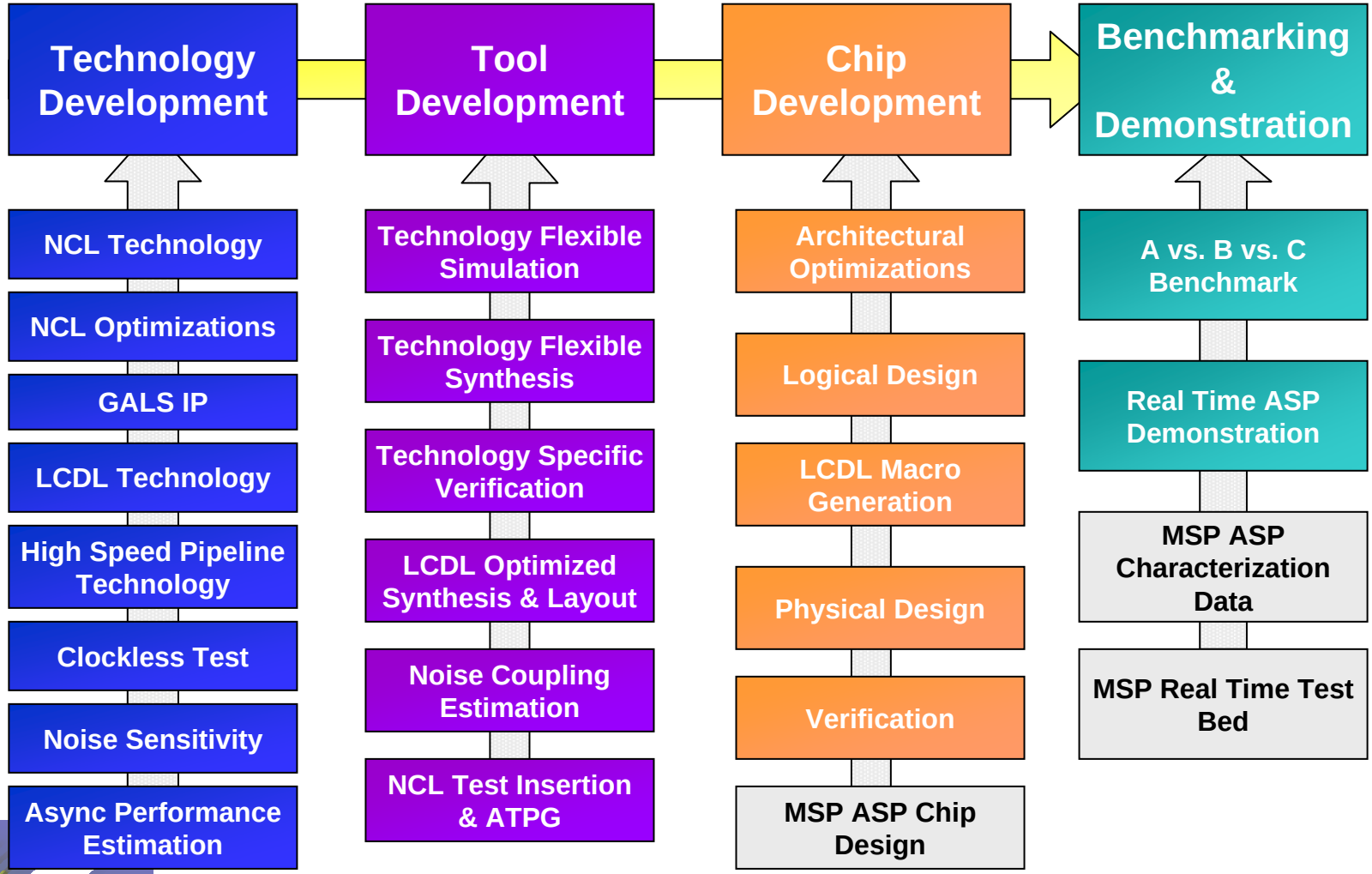
Minimum Learning Curve for Design Engineers
- Standard Languages

Compelling Demonstration
- Significant, Highly-constrained DoD Application

Address Concerns
- Noise Sensitivity
- Testability



Approach


Technology Development
Tool Development
Chip Development
Benchmarking & Demonstration
NCL Technology
NCL Optimizations
GALS IP
LCDL Technology
High Speed Pipeline Technology
Clockless Test
Noise Sensitivity
Async Performance Estimation
Technology Flexible Simulation
Technology Flexible Synthesis
Technology Specific Verification
LCDL Optimized Synthesis & Layout
Noise Coupling Estimation
NCL Test Insertion & ATPG
Architectural Optimizations
Logical Design
LCDL Macro Generation
Physical Design
Verification
MSP ASP Chip Design
A vs. B vs. C Benchmark
Real Time ASP Demonstration
MSP ASP Characterization Data
MSP Real Time Test Bed

Robust CAD Environment

- Provide Capability Equivalent to Industry Standard Design Flows
  - RTL to GDSII
  - Simulation & Verification
  - Physical Synthesis
  - Optimization
  - Multiple Clockless Styles
  - Test
- Commercially Available & Supported
  - Documentation
  - Training
  - Maintenance
- Compatible With Industry Standard Tools - Standard File Formats
  - VHDL
  - Cell Libraries
  - Placement Data
  - Netlists
- IP
  - GALS Blocks
  - Sync/Async Interfaces
- Proven
  - Silicon Verified Libraries
  - Demonstrated Results

Support for multiple clockless technologies

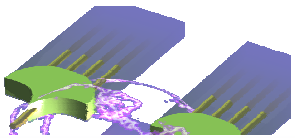
- Null Convention Logic (NCL)
- High-Speed Pipelines
- Locally Clocked Dynamic Logic (LCDL)
- Provides capability to trade off between performance, power, robustness, noise

Provide Significant Benefit

- Demonstrate significant improvement in critical parameters
  - Power
  - Performance
  - Design Time
  - Integration
  - Security
  - Robust Operation
- Provide parity in other critical parameters
- Ensure means to measure critical parameters
  - Including Noise Generation and Coupling
- Must show significant advantages to overcome inertia

Minimum Learning Curve

- Based on Standard Languages (VHDL, PSL)
- Compatible With Industry Standard Backend Tools
- Ability to Reuse Existing IP



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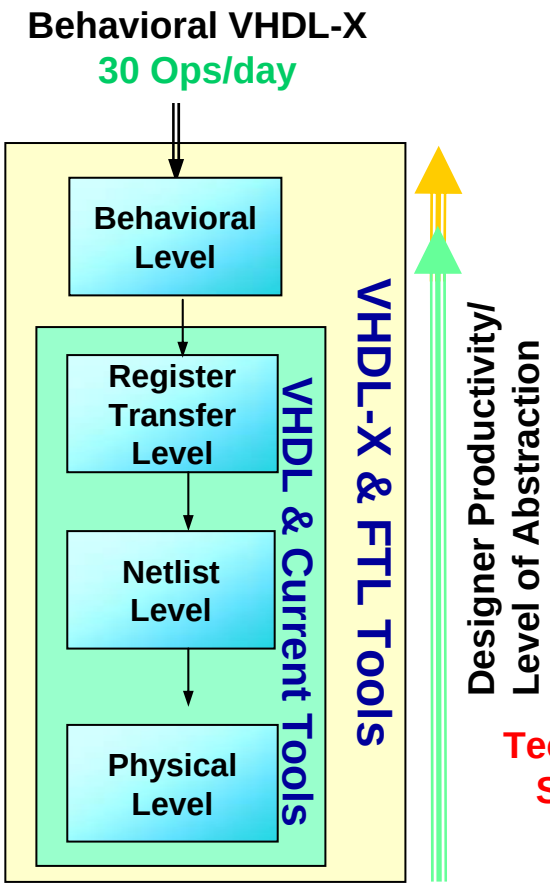
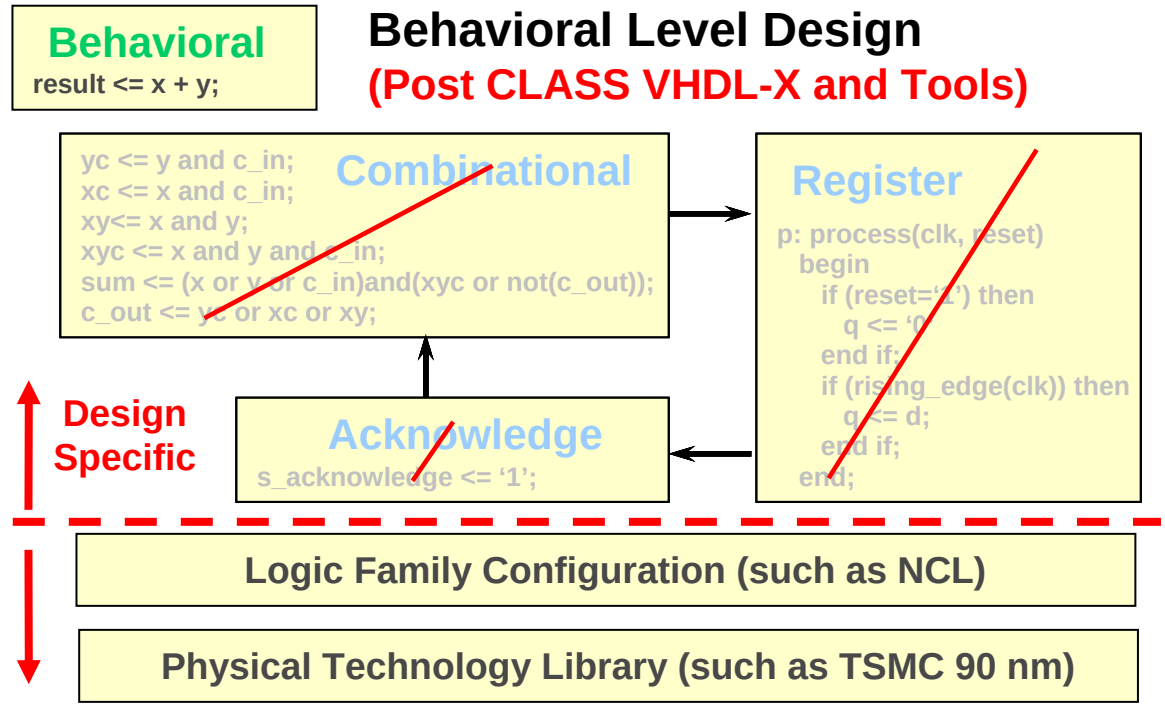
Compelling Demonstration

- Direct comparison between clocked and clockless
  - Based on MSP ASP chip
  - Identical Function
  - Identical Fabrication Process
  - Identical Measurement Methods
  - Demonstrated in MSP Real Time Test Bed
- Complex SoC Device
  - 10M gates
  - 25 Mbits SRAM
- Demonstrating Advanced Sensor Processor
  - Interesting to Multiple DoD Programs
  - Demonstrated Real Time Operation – Not previously achieved
- Studies to assess testability & noise sensitivity concerns and identify mitigation techniques

CLASS Tools
Improved Design Efficiency





VHDL-X abstracts logical technology

Eliminates need for detailed knowledge of clockless

abstracts "state" as registers and memory

Simplifies design specification, reduces code volume

abstracts data transactions and handshakes

Simplifies design specification, eliminates need for detailed clockless expertise

VHDL-X Enables Behavioral Level Design

Phase 1 Results
Logic Families - Macro Benchmarking
32-bit Adder

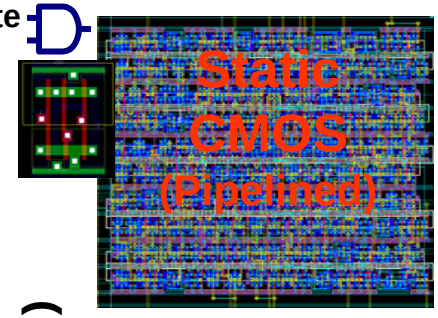
back

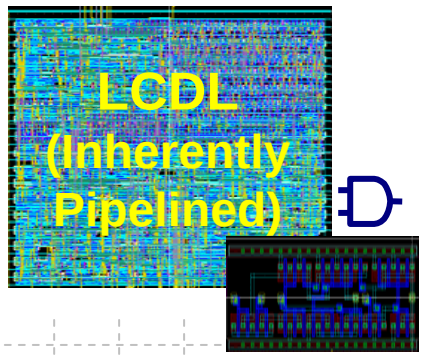
Best High Speed Family

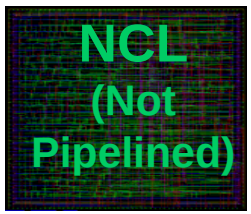
	Clockless					Clocked
	LCDL	Pulse-Based Logic with footer	PBL without footer	Asynchronous Differential Domino	Null Convention Logic (NCL)	Synchronous Static CMOS
Delay/Op	0.6 ns	0.5 ns	0.4 ns	2.4 ns	2.6 ns	1.5 ns
Power (at 384 MHz)	126 mW	367 mW	328 mW	122 mW	26 mW	346 mW
Power (at max throughput)	547 mW	1,906 mW	2,130 mW	133 mW	26 mW	600 mW
Energy/Op (independent of freq)	328 pJ	953 pJ	852 pJ	318 pJ	68 pJ	900 pJ

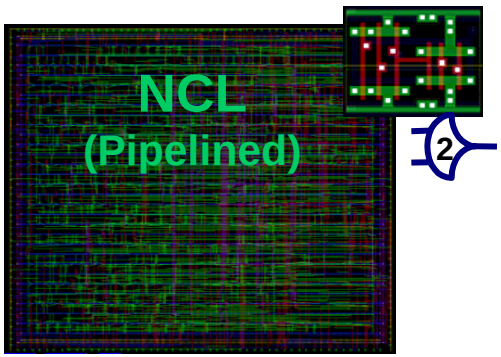
- Low Energy
- Delay Insensitive

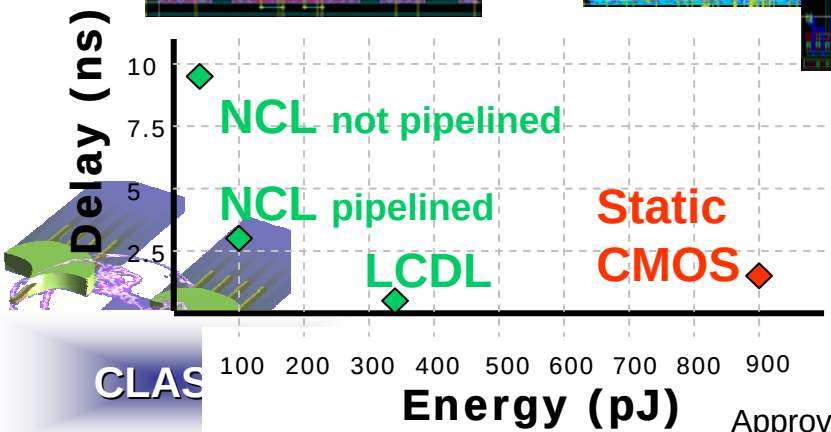
CMOS AND Gate

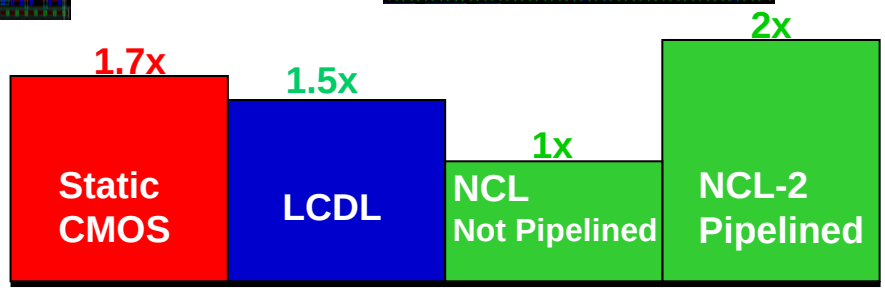












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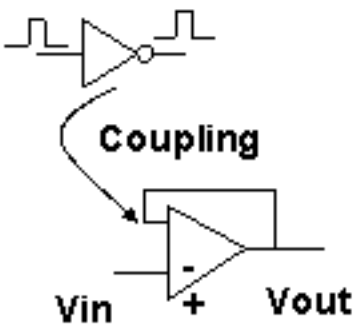
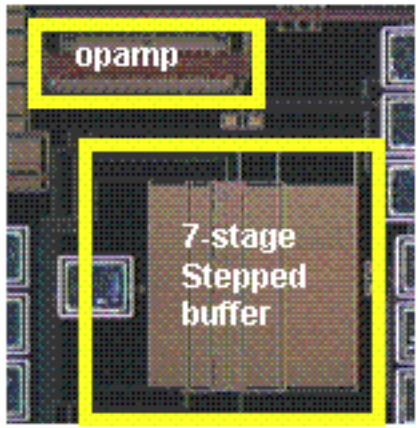
Substrate Noise Study Task (OSU)

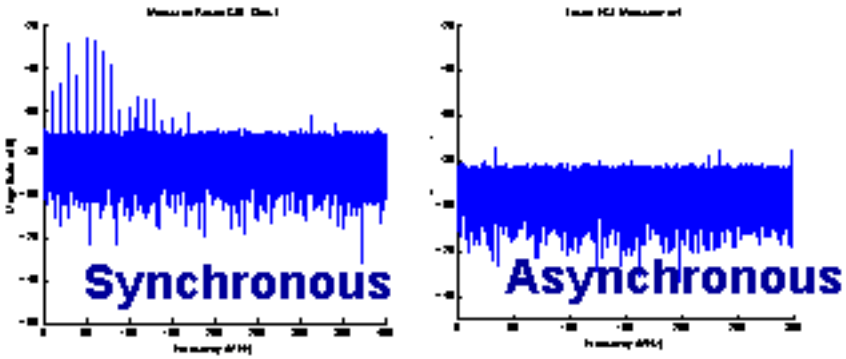
CLOCKED vs. CLOCKLESS MICROCONTROLLERS

- Compare Substrate Noise Generation of Clocked Logic and NCL in System-on-a-Chip Application
- Use Silencer! Substrate Noise Simulation Tool to Predict Noise and Validate Results with Test Chip





Substrate Noise Significantly Reduced in Asynchronous Implementation



Key Milestones

Milestone	Date
• Contract Award	6/17/04
• NCL & LCDL Library Test Chip Tape Out	1/28/05
• Production 10 Release	7/4/05
• LCDL Macros	5/1/05
• Optimized Logical Design	9/15/05
• Functional Verification/PDR	11/2/05
• Physical Design/CDR	6/3/06
• Parts on Dock	9/3/06
• Test & Characterization	10/30/06
• Real-Time Testbed Demonstration	10/30/06